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TITLE: Analog multiplier using emitter coupled transistor pair

OBJECTIVE: the students should be able to learn about Multiplier, Performance Parameter and characteristics.
APPLICATIONS: Piccolo - The 'sketching' Robot
UNIVERSITY QUESTIONS: 1. Explain the working of Analog multiplier using emitter coupled transistor pair. Discuss the applications of analog multiplier IC. (May/June-12) (16 Marks)

NOTES

2. What is two Quadrant Multiplier? (Nov/Dec-12) (2-marks)

3. Explain the working of an Analog multiplier using emitter coupled transistor with circuit diagram. (Nov/Dec-15) (16 Marks)

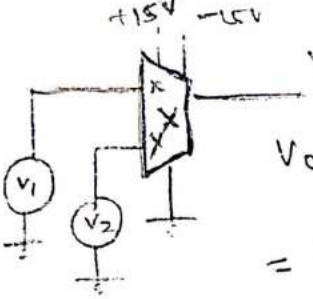
Introduction:-

* It is used to perform various mathematical operations. Simple and direct solution to complex signal processing problems.

output lead

Basic Multiplier and its characteristics

* Basic multiplier is an active circuit in which the o/p voltage is proportional to the product of the two input signals.



$$V_o = \frac{V_x V_y}{V_{ref}}$$

$$= K V_x V_y$$

the terminals v^+ and v^- are dual supply.

* The x and y are the two input terminal whereas two inputs V_1 and V_2 are connected.

The o/p of such basic multiplier is,

$$\boxed{V_o = K V_1 V_2} \quad \left[K = \frac{1}{V_{ref}}\right]$$

$(V_1 V_2 < V_{ref})$, the o/p of the basic multiplier will not saturate.

* Depending on the use of the basic multiplier it is necessary to restrict the polarity one (or) both the inputs.

* Depending on the polarity restrictions, the IC operation is called as.

1) One quadrant multiplier:-

In such operation, the polarities of both the inputs always be positive.

$(+V_1, +V_2 \rightarrow 1^{st}$ quadrant.)

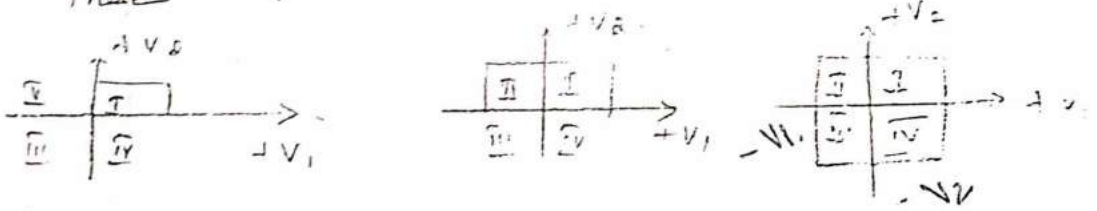
ii) Two Quadrant Multiplier: A two quadrant multiplier functions properly if one input is held positive and the other is allowed to swing in both positive and negative directions.

iii) Four Quadrant Multiplier: If both the inputs are allowed to swing in both positive and negative directions, the operation is four quadrant multiplier operation.

$V_1 \rightarrow +ve / -ve$

$V_2 \rightarrow +ve / -ve$

These operation are shown in fig.



PERFORMANCE PARAMETERS OF MULTIPLIER.

1. Accuracy:

It is the maximum deviation of the actual output lead from the ideal one. This deviation is also called total error. It is generally specified in terms of percentage of full scale output.

$\Rightarrow$ Total error = Ideal one − Max dev

It is specified in terms of %.

→ The Various [illegible]

the multipliers are..

(I) Logarithmic Amplifiers.

⇒ Max deviation from best fit straight line.

2. Linearity It is the maximum output deviation from the best fit straight line at the output where one input is varied from end to end, whilter the other is fixed.

3. Bandwidth

It is the range upto the frequency where the output is 3db below the low frequency value. This is also called small signal bandwidth. ⇒ upto frequency & below at low frequency small signal bandwidth 3db

4. Feed through Voltage:-

It is the peak to peak voltage at the output when one of the two input is grounded. As the output is the multiplication of the two inputs, if one of input is made zero, the output of ideal multiplier also must be zero.

$V_1 \to 0V$. Ideal Practical

$V_2 \to$ Some voltage 0V Some volt

→ But in pratice, there exists a small voltage at output, which is known as feed through voltage.

V_2 → gnd Ideal $V_0 = 0$ practical $V_0 \neq 0$

5. Zero trim (zero offset)

It is the ability of the multiplier to set the feed through voltages to get zero voltage at output. ⇒ Set the feed through voltage to set zero.

APPLICATIONS OF MULTIPLIER:

1. In Communication, it is used in amplitude modulation, phase modulation, frequency modulation, Phase detection, Suppressed carrier modulation etc

2. In Instrumentation and Control used to measure Velocity - acceleration, Instantaneous Power, Automatic gain Control etc.,

3. It is used for Voltage divider, True rms Calculation, rectifier, Phase shift detection etc,

4. It is used for frequency converters, frequency doubling and frequency shifting etc,

5. It is used for Squaring and Square root Calculations.

6. It is used to Solve nonlinear equations.

MULTIPLIER TECHNIQUES

→ The various techniques which are used for the multipliers are.

1. Logarithmic Amplifiers.
2. Quarter Square Multiplier
3. Pulse width / height Modulation Multipliers.

Suitable for monolithic IC realization. (1, 3, 4)

(4) Variable Transconductance Technique.

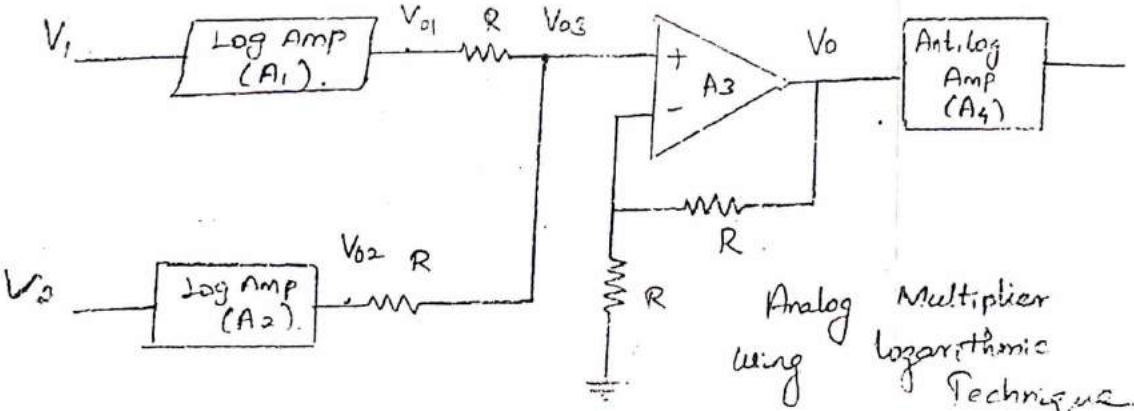
b) Current Rating Multipliers.

c) Triangle averaging multipliers.

→ Out of these techniques logarithmic, Pulse width/height modulation and Variable transconductance are suitable for monolithic IC realization of the multipliers.

LOGARITHMIC SUMMING TECHNIQUE

↳ Using log and antilog amplifiers, the circuit can be built to obtain the output proportional to the product of the two input voltages. The circuit is shown in fig.



Analog Multiplier using logarithmic Technique

⇒ The derivation for output of log and antilog amplifier is derived in chapter 2.

⇒ To get o/p ∝ Product of 2 input Voltage.

→ The o/p of log amplifier is given by

$$V_o = -K_1 \ln \frac{V_{in}}{I_{ref} R} \rightarrow (1)$$

where, $K_1 = \frac{V_T (R_1 + R_2)}{R_T}$

→ Similarly, the o/p of Antilog amplifier is given by

$$V_o = \frac{1}{K_2} \ln^{-1} \frac{V_{in}}{K_1}$$

where, $K_2 = \frac{1}{R I_{ref}}$

→ The log amplifiers A_1 and A_2 give the output V_{o1} and V_{o2}. From eqn (1), we may write the eqn for V_{o1} and V_{o2} as.

$$V_{o1} = -K_1 \ln \frac{V_1}{R I_{ref}}.$$

$$V_{o2} = -K_1 \ln \frac{V_2}{R I_{ref}}.$$

→ The opamp (A_3) is a non-inverting amplifier with unity gain. The o/p of A_3 is given by.

$$V_{o3} = V_{o1} + V_{o2}$$

$$= -K_1 \ln \frac{V_1}{I_{ref} R} - K_1 \ln \frac{V_2}{I_{ref} R}.$$

$$V_{o3} = -K_1 \ln \left[\frac{V_1 V_2}{(I_{ref} R)^2} \right] \rightarrow (3).$$

→ The output of A_3 is (V_{o3}) is applied to Op amp (A_4). A_4 is the antilog amplifier. The o/p of Antilog amplifier (V_o) can be written from eqn (2), we get.

$$V_o = \frac{-1}{K_2} \ln^{-1}\left[-K_1 \ln \frac{V_1 V_2}{(I_{ref} R)^2 \cdot K_1} \right]$$

$$\boxed{V_o = \frac{1}{K_2}\left[\frac{V_1 V_2}{(I_{ref} R)^2}\right]} \rightarrow (4).$$

→ Substitute the value, $K_2 = \frac{1}{I_{ref} R}$ in eqn (4). it becomes.

$$V_o = I_{ref} R \times \frac{V_1 V_2}{(I_{ref} R)^2} = \frac{V_1 V_2}{I_{ref} R}.$$

$$V_o = \frac{V_1 V_2}{V_{ref}} \text{ (or) } K_2 V_1 V_2.$$

∴ The output of an analog multiplier is.

$$\boxed{V_o = K_2 V_1 V_2 = \frac{V_1 V_2}{I_{ref} R} \text{ (or) } \frac{V_1 V_2}{V_{ref}}.}$$

MULTIPLIER USING AN EMITTER COUPLED TRANSISTOR PAIR.

→ A Circuit using an emitter Coupled pair is shown in fig. The output currents I_{C1} and I_{C2} are related to the differential input voltage (V_1) by.

$$I_{C1} = \frac{I_{EE}}{1+e^{-V_1/V_T}} \rightarrow (1)$$

$$I_{C2} = \frac{I_{EE}}{1+e^{+V_1/V_T}} \rightarrow (2)$$

→ Where, V_T is the thermal Voltage and the base Current has been neglected. V_1 → i/p Voltage

→ Combining Eqn (1) & (2), we have the difference between the two output Current as

$$\Delta I_C = I_{C1} - I_{C2} \rightarrow (3).$$

$$= I_{EE}\left[\frac{1}{1+e^{-V_1/V_T}} - \frac{1}{1+e^{+V_1/V_T}}\right]$$

$$\Delta I_C = I_{EE} \tanh\left[\frac{V_1}{2V_T}\right] \rightarrow (4).$$

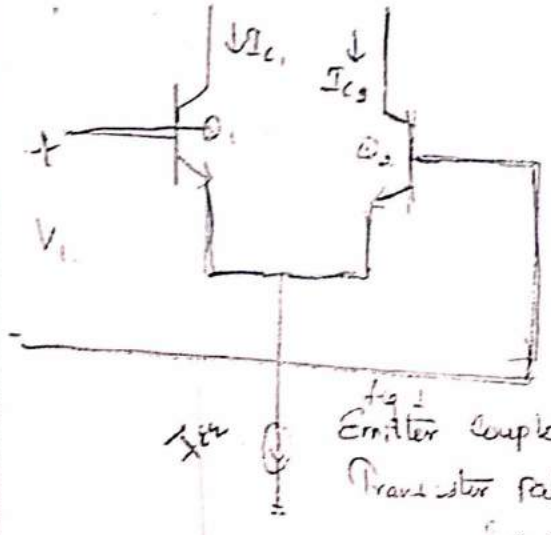


fig 1 Emitter Coupled Transistor pair

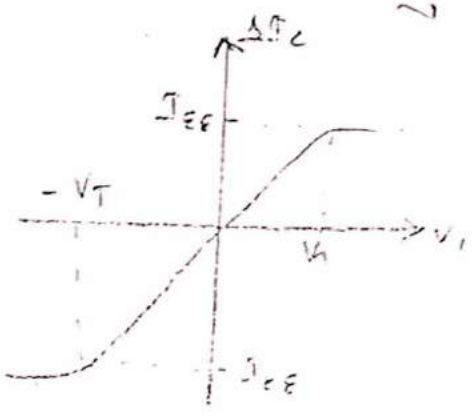


fig 2. DC transfer characteristics

in the Gilbert cell (2). V_2 must be always p...
results in only a two-quadrant multiplier operation. ($V_1 \rightarrow +ve | -ve$)
& $\tanh(x)$ is approximated as x, where

→ The dc transfer characteristics of the emitter coupled pair is shown in fig(2). It shows that the emitter coupled pair can be used as a simple multiplier using this configuration.

→ When the differential input voltage, $V_1 << V_T$, we can approximate as given by.

$$I_{EE} \tanh\left(\frac{V_1}{2V_T}\right) \approx I_{EE}\left(\frac{V_1}{2V_T}\right) \rightarrow (5).$$

Then Eqn (4) becomes.

$$\Delta I_C = I_{EE}\left(\frac{V_1}{2V_T}\right) \rightarrow (6).$$

→ The current (I_{EE}) is the bias current for the emitter coupled transistor pair. If the current (I_{EE}) is made proportational to the second input signal V_2, then. $I_{EE} \propto V_2$

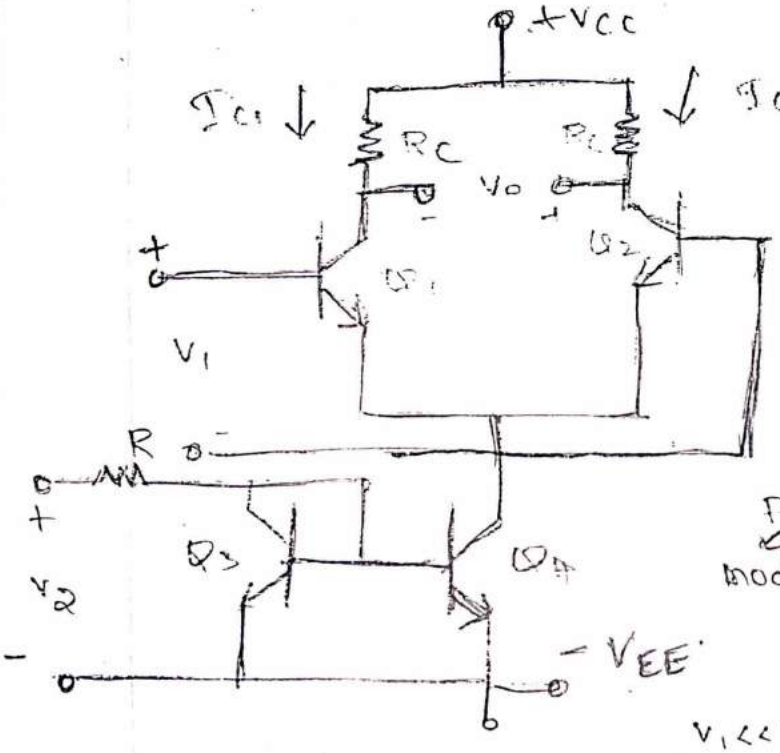
$$I_{EE} = K_0 (V_2 - V_{BE\,ON}) \rightarrow (7).$$

→ Substituting the value I_{EE} in eqn (6), we get.

$$\Delta I_C = \frac{K_0 V_1 (V_2 - V_{BE(ON)})}{2V_T}, \rightarrow (8).$$

↳ This arrangement is shown in fig(3)

It is a simple modulator circuit. It can be used as a multiplier, provided V_1 is small and much less than 50mV, and V_2 is greater than V_{BE} (on). But the multiplier circuit shown in fig(3) has several limitations.



$V_1 < 50mV$

$V_2 > V_{BE}(on)$

Fig: A simple modulator using differential Amplifier

$V_1 << V_T$

In room temp $V_T = 26$ V_T is very small to satis

Limitations:-

(This limitations are overcome in the Gilbert cell)

1. V_2 is offset by $V_{BE}(on)$, the approximation
2. V_2 must be always positive, which results in only a two-quadrant multiplier operation. ($V_1 \rightarrow +ve / -ve$)
3. $\tanh(x)$ is approximated as x, where

$$x = \frac{V_1}{2V_T}$$

Key Points :-

* Basic multiplier and its characteristics
* Performance Parameters of multiplier
* Applications of multiplier
* Multiplier Techniques.

$$V_{01} = -K_1 \ln \frac{V_1}{R I_{ref}}$$

$$V_{02} = -K_1 \ln \frac{V_2}{R \cdot I_{ref}}$$

$$V_{03} = -K_1 \ln \left[\frac{V_1 V_2}{(I_{ref} \cdot R)^2} \right]$$

$$V_0 = K_2 V_1 V_2 = \frac{V_1 V_2}{I_{ref} \cdot R}$$

$$\Delta I_C = \frac{K_0 V_1 (V_2 - V_{BE(ON)})}{2 V_T}$$

TITLE: Gilbert Multiplier Cell

OBJECTIVE: The students should be able to learn about Gilbert multiplier cell and Predistortion circuit.

APPLICATIONS:

Lytro light Field Camera

UNIVERSITY QUESTIONS:

1. Under what conditions will the Gilbert cell function as a multiplier? (Apr/May-15) (2marks)

Gilbert Multiplier Cell: NOTES

* The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four quadrant multiplication.
* It forms the basis of most of the Integrated circuit balanced multiplier.
* Two cross coupled emitter coupled emitter coupled pairs in series connection with an emitter coupled pair from the structure of Gilbert multiplier cell

The collector currents of Q_3 and Q_4 are given by,

$$I_{C3} = \frac{I_{C1}}{1 + e^{-V_1/V_T}} \longrightarrow (1)$$

and

$$I_{C4} = \frac{I_{C1}}{1 + e^{V_1/V_T}} \longrightarrow (2)$$

Similarly, the collector currents I_{C1} and I_{C2} of transistors Q_1 and Q_2 can be expressed as,

$$I_{C5} = \frac{I_{C2}}{1 + e^{V_1/V_T}} \longrightarrow (3)$$

and

$$I_{C6} = \frac{I_{C2}}{1 + e^{-V_1/V_T}} \longrightarrow (4)$$

→ The collector currents I_{C_1} and I_{C_2} of transistors (Q_1 and Q_2) can be expressed as

$$I_{C_1} = \frac{I_{EE}}{1+e^{-V_2/V_T}} \quad \rightarrow (5).$$

$$\& \quad I_{C_2} = \frac{I_{EE}}{1+e^{V_2/V_T}} \quad \rightarrow (6).$$

→ Substituting eqn (6) in eqn (1) & (2), we get.

$$I_{C_3} = \frac{I_{EE}}{\left[1+e^{-V_1/V_T}\right]\left[1+e^{-V_2/V_T}\right]} \quad \rightarrow (7).$$

$$\& \quad I_{C_4} = \frac{I_{EE}}{\left[1+e^{V_1/V_T}\right]\left[1+e^{-V_2/V_T}\right]} \quad \rightarrow (8).$$

→ Illy., Substituting eqn (6) in eqn (3) & (4), we get

$$I_{C_5} = \frac{I_{EE}}{\left[1+e^{V_1/V_T}\right]\left[1+e^{V_2/V_T}\right]} \quad \rightarrow (9).$$

$$\& \quad I_{C_6} = \frac{I_{EE}}{\left[1+e^{-V_1/V_T}\right]\left[1+e^{V_2/V_T}\right]} \quad \rightarrow (10).$$

→ The differential output current (ΔI) is given by.

$$\Delta I = I_{L_1} - I_{L_2}.$$

i.e. $$\Delta I = (I_{C_3} + I_{C_5}) - (I_{C_4} + I_{C_6}).$$

(or) $$\Delta I = (I_{C_3} - I_{C_6}) - (I_{C_4} - I_{C_5}) \quad \rightarrow (11).$$

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* The above equ is reffered from the equ

$$I_{EE} = K_0(V_2 - V_{BE\,ON})$$ *

* The current (I_{EE}) is the bias current for the emitter coupled pair.

* In equ (1) & (2) the I_{01} is the dc current flowing in each o/p, K_1 is the transconductance of the V-I Converter, and it is assumed that $V_1 = 0$

* The differential voltage ΔV across the diode connected transistor Q_7 and Q_8 is given by,

$$\Delta V = V_T \ln\left(\frac{I_{01} + K_1 V_1}{I_0}\right) - V_T \ln\left(\frac{I_{01} - K_1 V_1}{I_0}\right) \rightarrow (3)$$

Basic log amplifier is.

$V_0 = V_i \ln \frac{I_F}{I_i}$ X, the equ (3) is derived,

we may write the equ (3) as,

$$\Delta V_1 = V_T \ln\left[\frac{I_{01} + K_1 V_1}{I_{01} - K_1 V_1}\right] = V_T \ln\left[\frac{1 + \frac{K_1 V_1}{I_{01}}}{1 - \frac{K_1 V}{I_{01}}}\right]$$

This can be transformed into

$$\Delta V_1 = 2 V_T \tanh^{-1}\left[\frac{K_1 V_1}{I_{01}}\right] \rightarrow (4)$$

$$\tanh^{-1}(x) = \frac{1}{2} \ln\left(\frac{1+x}{1-x}\right)$$

→ formula

we may write the equ (4)

$$\tanh\left(\frac{\Delta V_1}{2V_T}\right) = \left[\frac{K_1 V_1}{I_{O1}}\right] \rightarrow (5)$$

Ily we have to write the equ for the i/p voltage (V_2) is applied.

$$\tanh\left(\frac{\Delta V_2}{2V_T}\right) = \left[\frac{K_2 V_2}{I_{O2}}\right] \rightarrow (6)$$

equ (5) & (6) is applied on equ (3)

$$\Delta I = I_{EE}\left[\frac{K_1 V_1}{I_{O1}}\right]\left[\frac{K_2 V_2}{I_{O2}}\right] \rightarrow (7)$$

I_{O1}, $K_1 I_{O2}$, K_2 - Functional block parameters

V_1, V_2 - I/p's.

equ (7) shows that the differential o/p is proportional to the product $V_1 V_2$.

* Hence the inverse hyperbolic tangent block compensates for the non-linearity of the i/p's.

Key Points:-

* Gilbert multiplier cell
* Gilbert multiplier with predistortion cells

$$\Delta I = I_{EE}\left[\tanh\left(\frac{V_1}{2V_T}\right)\tanh\left(\frac{V_2}{2V_T}\right)\right]$$

$$\Delta I = I_{EE}\left[\frac{K_1 V_1}{I_{O1}}\right]\left[\frac{K_2 V_2}{I_{O2}}\right]$$

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TITLE: Four Quadrant Analog multiplier

OBJECTIVE: The students should be able to learn about 4-Quadrant analog multiplier.

APPLICATIONS:

Lytro light field camera.

UNIVERSITY QUESTIONS:

1. Explain about four Quadrant analog multiplier

NOTES

Four Quadrant Analog multiplier :-

The complete four quadrant Analog multiplier circuit using Gilbert cell is shown in figure.

→ The three boxes are Voltage to Current 18.3
Converter (or) Current to Voltage Converters in effect.

→ The predistortion for the input signal is achieved by transistor Q_7 and Q_8.

→ The current I_9 and I_{10} passing through the emitters of Q_7 and Q_8 generate a voltage between the two emitter terminals, that is Proportional to the inverse hyperbolic tangent of V_1. (i.e $\tanh^{-1}$)

→ This compensates for the hyperbolic tangent expression for Eqn (12).

ANALYSIS OF THE CIRCUIT

→ The Currents through base emitter junctions of transistors Q_7, Q_3, Q_4 and Q_8 Connected in Series can be expressed by.

$$I_9 I_3 = I_4 I_{10} \rightarrow (1).$$

→ 118, from the series connection of the transistors Q_7, Q_6, Q_5 and Q_8, we get.

$$I_9 I_6 = I_5 I_{10} \rightarrow (2).$$

→ From fig, we see that

$$I_1 = I_3 + I_4 \rightarrow (3)$$

$$I_2 = I_5 + I_6 \rightarrow (4)$$

$$I_{L1} = I_3 + I_5 \rightarrow (5)$$

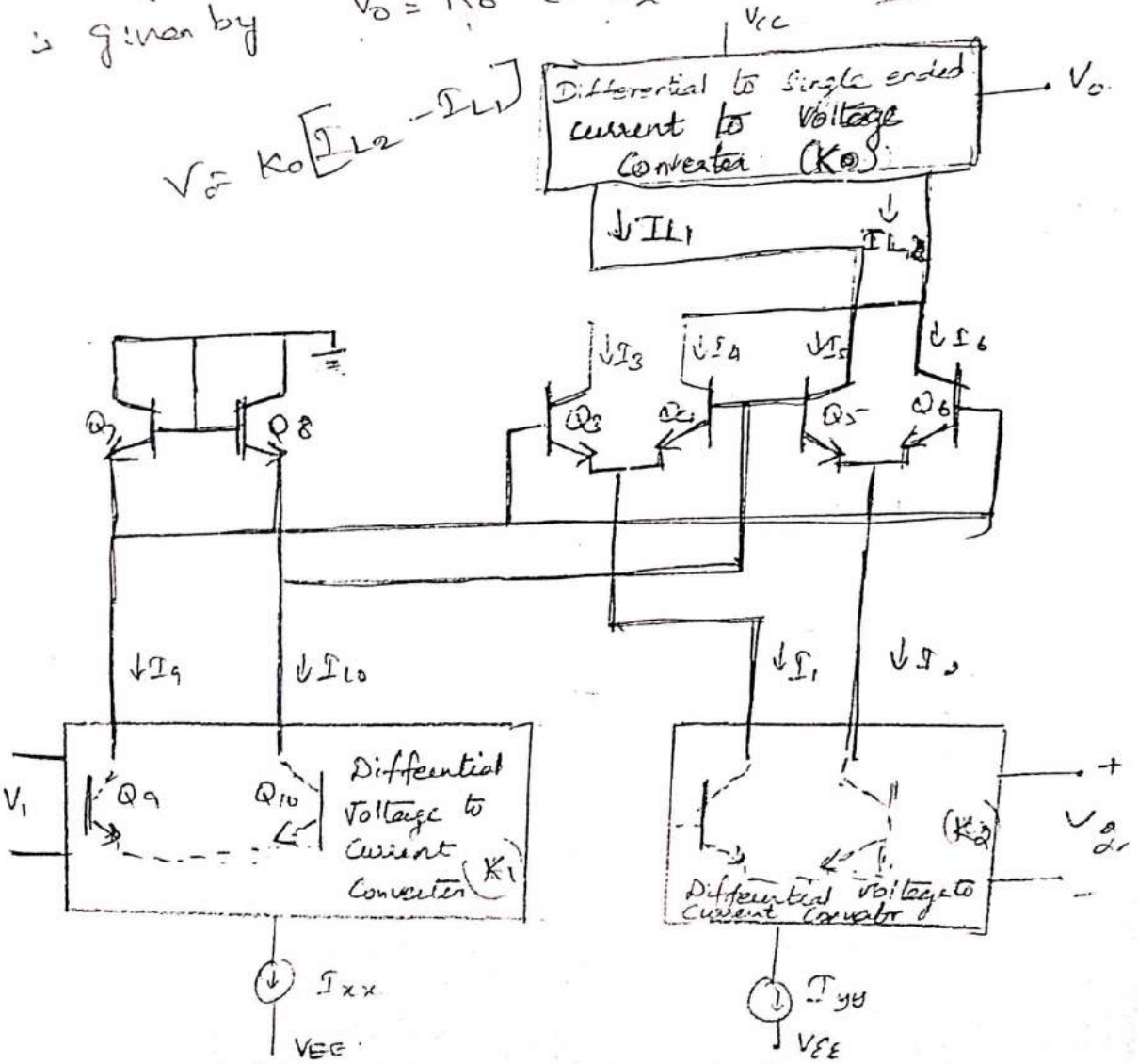
$$I_{L2} = I_4 + I_6 \rightarrow (6)$$

& $I_{xx} = I_9 + I_{10} \rightarrow (7)$

→ The transfer characteristics of the differential to single ended current to voltage converter is given by

$$V_o = K_o (I_{L2} - I_{L1}) \rightarrow (8)$$

$$V_o = K_o [I_{L2} - I_{L1}]$$



$I_6 = I_5 \times \frac{I_{10}}{I_9}$.

$= I_A \times \frac{I_{10}}{I_9}$.

→ The transfer characteristics of the differential voltage to current converter is given by

$I_9 - I_{10} = V_1/K_1 \rightarrow (9)$.

$I_1 - I_2 = V_2/K_2 \rightarrow (10)$.

where K_0, K_1 & K_2 are constants.

→ Substituting for I_{L1} & I_{L2} from eqn (5) & (6) in eqn (8), we get.

$V_0 = K_0 [(I_4 + I_6) - (I_3 + I_5)]$

using Eqn (1) & (2),

$V_0 = K_0 \left[\left(I_4 + I_5 \times \frac{I_{10}}{I_9} \right) - \left(I_4 \times \frac{I_{10}}{I_9} + I_5 \right) \right]$

Simplifying the above eqn, we get.

$V_0 = K_0 \left[(I_4 - I_5) - \left(I_4 \times \frac{I_{10}}{I_9} - I_5 \times \frac{I_{10}}{I_9} \right) \right]$.

$= K_0 \left[(I_4 - I_5) - \frac{I_{10}}{I_9} (I_4 - I_5) \right]$.

$= K_0 (I_4 - I_5) \left[1 - \frac{I_{10}}{I_9} \right]$.

$$\boxed{V_0 = K_0 (I_4 - I_5) \left(\frac{I_9 - I_{10}}{I_9} \right)} \rightarrow (12).$$

from fig, we see that.

$I_1 - I_2 = (I_3 + I_4) - (I_5 + I_6) \rightarrow (13)$.

using Eqn (1) & (2), we get

$$I_1 - I_2 = \left(I_4 \times \frac{I_{10}}{I_9} + I_4 \right) - \left(I_5 + I_5 \times \frac{I_{10}}{I_9} \right)$$

Solving $(I_4 - I_5)$ from above eqn.

$$= I_4 \left[1 + \frac{I_{10}}{I_9} \right] - I_5 \left[1 + \frac{I_{10}}{I_9} \right]$$

$$I_1 - I_2 = \left(\frac{I_9 + I_{10}}{I_9} \right) (I_4 - I_5).$$

$$(I_4 - I_5) = (I_1 - I_2) \times \left(\frac{I_9}{I_9 + I_{10}} \right) \rightarrow (14).$$

Substitute Eqn (14) in Eqn (12), it becomes.

$$V_0 = K_0 (I_1 - I_2) \times \frac{\cancel{I_9}}{I_9 + I_{10}} \times \frac{I_9 - I_{10}}{\cancel{I_9}}$$

$$V_0 = K_0 (I_1 - I_2) \frac{(I_9 - I_{10})}{I_9 + I_{10}} \rightarrow (15).$$

$I_9 + I_{10} = I_{xx}$

$I_9 - I_{10} = V_1/K_1$

$I_1 - I_2 = \frac{V_2}{K_2}$

using Eqn 07, 9, 10 & in Eqn (15).

$$\boxed{V_0 = \frac{K_0 \, V_1 V_2}{I_{xx} K_1 K_2} = K_m V_1 V_2} \rightarrow (16).$$

$$\boxed{K_m = \frac{K_0}{I_{xx} K_1 K_2}}$$

→ In Eqn (16) has no approximation. Hence, the input signal amplitudes have no constraints.

TITLE: Variable Trans conductance technique

OBJECTIVE: The student should be able to learn about 4 - quadrant variable transconductance technique.
APPLICATIONS: Tosiba FGMOS Transistor.
UNIVERSITY QUESTIONS:

1. Explain the operation of a variable transconductance multiplier. (Nov/Dec-16) (16 marks)

NOTES

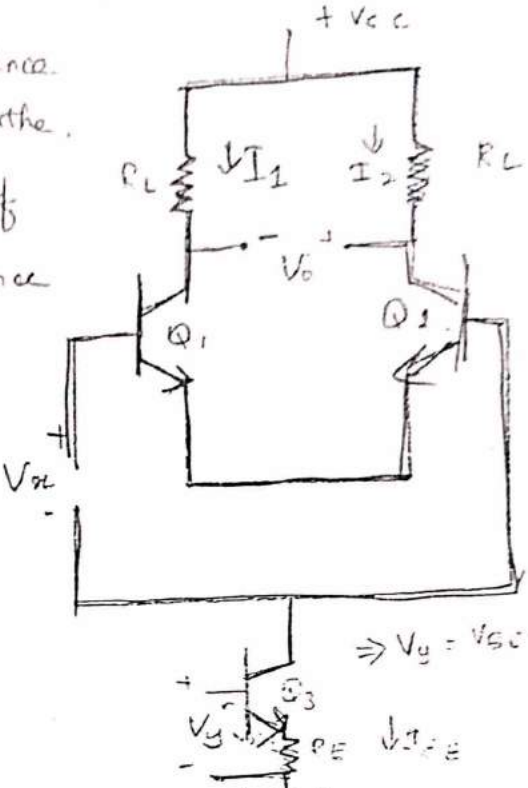
2. Explain, with necessary equations, the basic circuits of 'linearized transconductance multiplier' and differential V-I Converter' Hence explain the 'Four quadrant variable transconductance multiplier' circuit.

(Nov/Dec-12) (16-marks)

$$V_o = K_o \cdot \frac{V_1 V_2}{I_{xx} K_1 K_2}$$

VARIABLE TRANSCONDUCTANCE TECHNIQUE

→ The Variable Transconductance technique make use of the dependence characteristics of the transistor transconductance parameter on the emitter current bias applied.



→ A simple circuit arrangement is shown in fig is working under this principle.

→ The principle V_o and V_x is given by.

$$\boxed{V_o = g_m R_L V_x} \rightarrow (1)$$

Where $g_m = I_{EE} / V_T$ is the transconductance of the stage.

→ Application of second input (V_y) to the reference current source (I_{EE}) of the differential amplifier can vary g_m.

from fig, we may write.

$$V_y = V_{BE} + I_{EE} R_E \quad ; \quad \text{If } V_{BE} << I_{EE} R_E.$$

the eqn becomes.

$$V_y = I_{EE} R_E$$

$$I_{EE} = \frac{V_y}{R_E} \rightarrow (2)$$

The eqn (2) is applied in eqn (1), it becomes.

$$V_o = \frac{V_y}{R_E \cdot V_T} \times R_L \times V_x.$$

$$\left\{ g_m = I_{EE}/V_T. = \frac{V_y}{R_E V_T} \right\}.$$

$$\boxed{V_o = \frac{R_L}{R_E V_T} V_x V_y}$$

Generation of logarithmic Bias input for Differential Stage:

→ The linearized transconductance multiplier is the heart of the four quadrant Variable transconductance multiplier circuit.

→ The linearised transconductance multiplier is shown in Fig(2).

→ The Collector Currents (I_1) and (I_2) are related to the applied Voltage (V_x) by the relation

$$\frac{I_1}{I_2} = e^{(V_x/V_y)} \rightarrow (3)$$

→ Therefore, Linearity can be achieved by reducing the exponential current - voltage characteristics to a linear one as shown in fig.

→ The transistor Q_1 and Q_2 are biased through the diode connected Q_A and Q_B, which are driven by controlled current sources (I_A & I_B) respectively. Then the net bias voltage (V_x) is represented by.

$$V_x = V_T \ln (I_B/I_A) \rightarrow (2).$$

Substituting Eqn (2) in Eqn (1)

$$\frac{I_1}{I_2} = e^{(V_x/V_T \ln I_B/I_A/V_T)}.$$

$$= I_B/I_A \quad \left[\begin{array}{l} \text{where } V_T \text{ is less.} \\ V_T >> V_x. \text{ Hence, they} \\ \text{are neglected} \end{array}\right.$$

$$\therefore \frac{I_1}{I_2} = \frac{I_B}{I_A}.$$

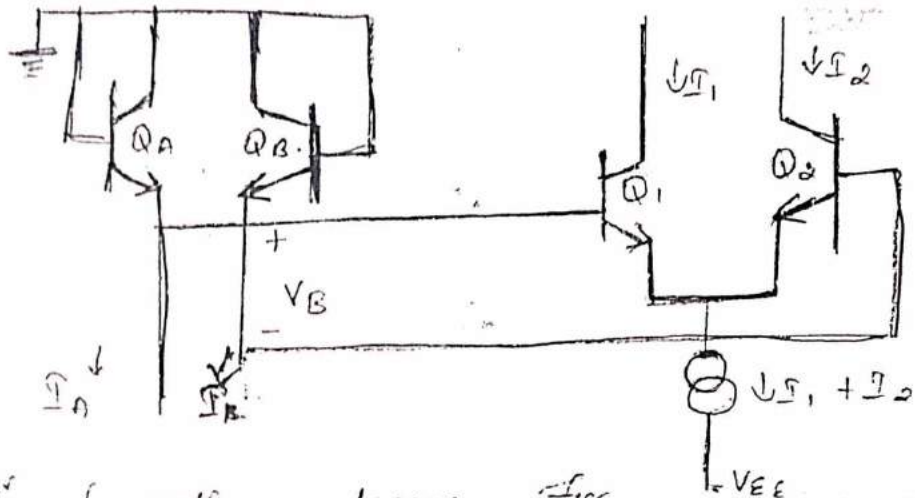
we may write;

$$1 + \frac{I_1}{I_2} = 1 + \frac{I_B}{I_A} = 1 + e^{V_x/V_T}.$$

$$\frac{I_2 + I_1}{I_2} = \frac{I_A + I_B}{I_A} = 1 + e^{V_x/V_T}.$$

$$\boxed{\frac{I_2}{I_2 + I_1} = \frac{I_A}{I_A + I_B} = \frac{1}{1 + e^{V_x/V_T}}} \rightarrow (3).$$

$$\boxed{\frac{I_B}{I_A + I_B} = \frac{I_1}{I_1 + I_2} = \frac{e^{V_x/V_T}}{1 + e^{V_x/V_T}}} \rightarrow (4)$$



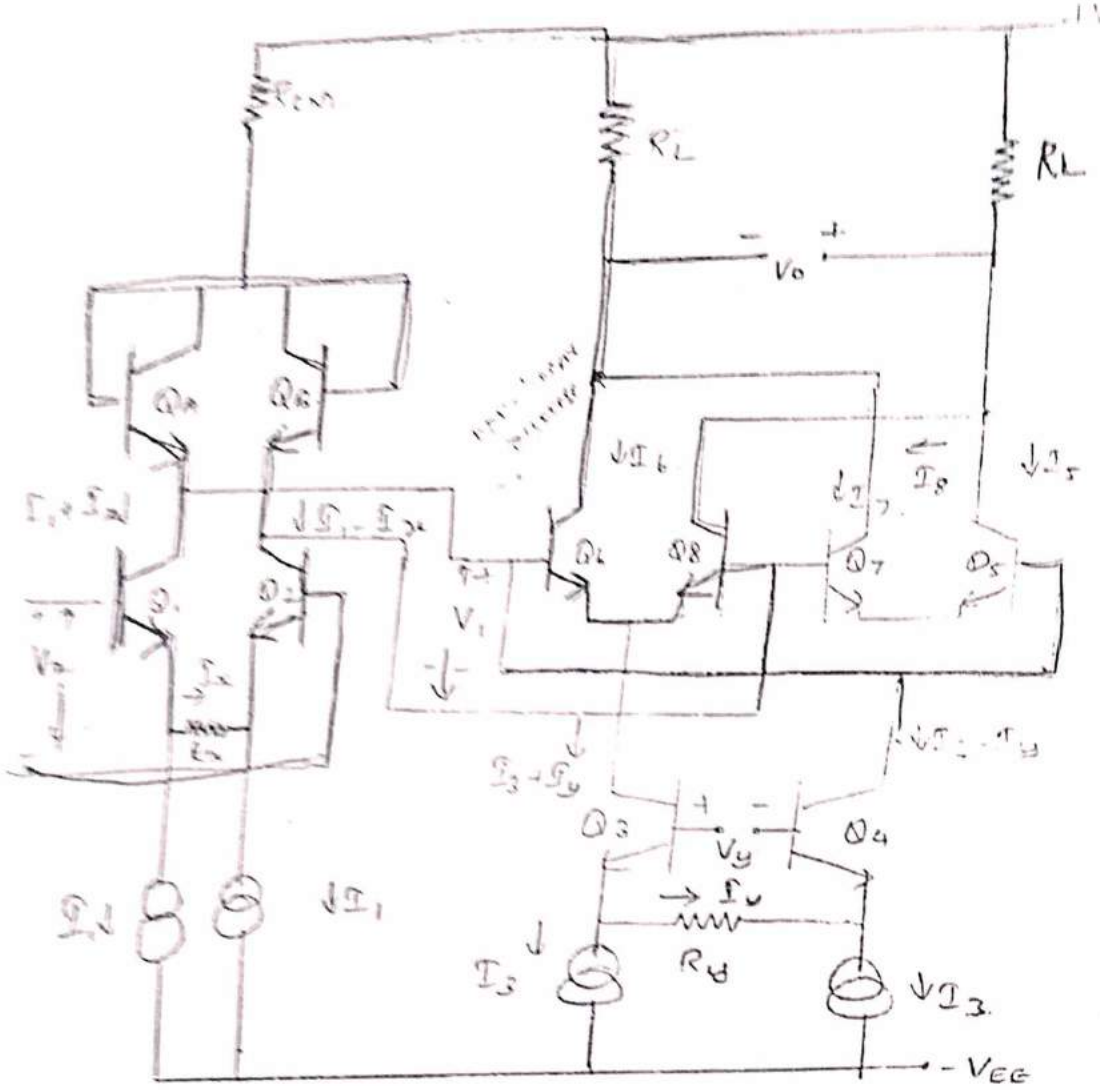
Adv Logarithmic biasing for increasing linearity of multiplier.

→ The above equations are valid over a wider range. If the device characteristics are well matched and V_{BE} obeys the basic diode equation.

FOUR QUARDANT VARIABLE TRANSCONDUCTANE AMPLIFIER:

→ A typical four quadrant multiplier circuit is shown in fig (3). The four quadrant operation indicates that the voltage is directly proportational to the product of the two input voltages regardless of the polarity of the inputs and such multiplier can be

in all the four quadrants of operation.



four quadrant multiplier using

1. V_1 generate
   Q_A & Q_B by V_x Variable Transconductance
2. V_1 → nonlinear. Technique
   to
   linear by Q_5 Q_6 Q_7 Q_8 Tr pair
3. R_x, R_y → Regeneration resistor to I/p
   Provide linear i/p Voltage

Page 6 of 9

→ The first part of the circuit generates an intermediate voltage V_1 across the transistors Q_4 and Q_8 in response to the input signal V_x.

→ The non linear response to the input V_x in generating V_1 is compensated by the inverse non-linearity associated with the base emitter junction of the quad-transistors $Q_5 - Q_6$ and $Q_7 - Q_8$. Thus the output voltage (V_o) is maintained proportional to the linear product of the two input voltages.

→ The emitter degeneration resistor R_x and R_y provide linear conversion of the input voltages to differential currents I_x and I_y.

→ Thus $I_x = \frac{V_x}{R_x}$ and $I_y = \frac{V_y}{R_y}$. The value of R_x and R_y are chosen such that $R_x >> V_T/I_1$ and $R_y >> V_T/I_2$ respectively.

→ The output voltage (V_o) can be written as.

$$V_o = R_L \left[(I_6 + I_7) - (I_5 + I_8) \right] \rightarrow (5).$$

'omparing the fig 2 and fig 3, the equ ③ & ④ is applied to the fig 3, we obtain

Fig 2 → Fig 3

$I_3 \rightarrow I_5$

$I_1 \rightarrow I_6$

$I_2 \rightarrow I_1 + I_2$

$I_3 \rightarrow I_1 - I_2$

$V_1 \rightarrow V_x$

$I_1 + I_2 \rightarrow I_2 - I$

Q6 = $\frac{I_6}{I_3 + I_y} = \frac{I_5}{I_3 - I_y} = \frac{I_1 + I_x}{2I_1} \rightarrow (6)$ (Q5, Q1)

Q8 $\frac{I_8}{I_3 + I_y} = \frac{I_7}{I_3 - I_y} = \frac{I_1 - I_x}{2I_1} \rightarrow (7)$ (Q4, Q2)

The I_5, I_6, I_7, I_8 are determined by equ ⑥ & ⑦ then.

this value is substituted in equ ⑤ we get

$$V_o = R_L \left[\left(\frac{I_1 + I_x}{2I_1} \times (I_3 + I_y) + \frac{I_1 - I_x}{2I_1} (I_2 - I_y) \right) \right.$$

$$\left. - \left(\frac{I_1 + I_x}{2I_1} (I_3 - I_y) + \frac{I_1 - I_x}{2I_1} (I_3 + I_y) \right) \right]$$

$$= \frac{R_L}{2I_1} \left[\left(I_1 I_3 + I_x I_3 + I_1 I_y + I_x I_y + I_1 I_3 - I_x I_3 - I_1 I_y + I_x I_y \right) - \right.$$

$$\left. \left(I_1 I_3 + I_x I_3 - I_1 I_y - I_x I_y + I_1 I_3 - I_x I_3 + I_1 I_y - I_x I_y \right) \right]$$

$$= \frac{R_L}{2I_1} \left[2I_1 I_3 + 2 I_x I_y - 2I_1 I_3 + 2 I_x I_y \right]$$

$$V_o = \frac{R_L}{2I_1} \times 4 I_x I_y = \frac{2 R_L}{I_1} I_x I_y$$

$$V_o = \frac{2R_L}{I_1} I_x I_y \rightarrow 8$$

I_x and I_y are linearly related to V_x & V_y respectively; we have

$$V_o = K V_x V_y \cdot$$

[where $I_x = V_x / R_x$
$I_y = V_y / R_y$

Scaling factor $K = \frac{2R_L}{I_1 R_x R_y}$

which is normally chosen as 0.1

Key Points :-

* variable transconductance

$$V_o = g_m R_L V_x$$

* f - variable transconductance

$$V_o = \frac{2R_L}{I_1} I_x I_y.$$

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TITLE: Analog multiplier applications

OBJECTIVE: The students should be able to learn about voltage divider, squaring circuit, square rooting etc.

APPLICATIONS:
Carbon nanotube field effect transistor (CNFET)

UNIVERSITY QUESTIONS:

1. Discuss the Applications of analog multiplier ICs (May/June-13) (16 marks)
2. How do you Convert a basic multiplier to a squaring and square root circuit (Apr/May-15) (5 marks)
3. Explain the working of a divider circuit using multiplier IC. (Nov/Dec-13) (16 marks

NOTES

Analog multiplier Applications :-

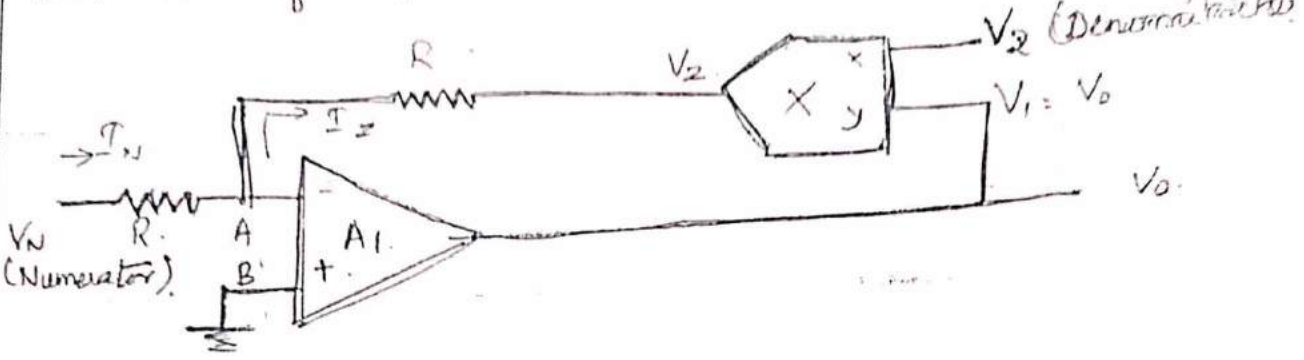
* Voltage divider ($\frac{V}{V}$)
* Squaring circuit (V^2)
* Square rooting circuit ($\sqrt{V}$)
* Frequency doubler (2ω)
* phase angle detection ($\phi = ?$)

Voltage divider :-

* The circuit in which output is the divison of the two input signals is called as a "divider".

* The multiplier is used in the feedback loop the denominator is applied at the x input of the multiplier, which is the voltage (V_2).

→ The numerator is applied at the input terminal of op-amp A_1.



→ As node A is generated, node B is also at Virtual ground, hence $V_A = 0$. As opamp input current is zero.

$$\left\{ I_N = \frac{V_N}{R} \quad I_Z = \frac{-V_Z}{R} \right\}$$

$$I_N = I_Z = \frac{V_N}{R} = -\frac{V_Z}{R}$$

$$V_Z = K V_1 V_2 = K V_0 V_2 \qquad \{ V_1 = V_0 \}$$

$$\frac{V_N}{R} = \frac{-K V_0 V_2}{R}$$

$$\boxed{V_0 = -\frac{V_N}{K V_2}}$$

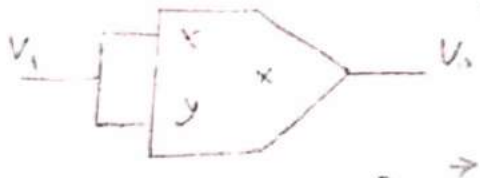
→ i/p (Nr) division of i/p ⊿
→ i/p (dr) $V_1 \to +ve$, $V_2 \to -ve$
2nd Qua

→ Thus, the output is proportational to the division of the two input voltages V_N and V_2.

→ The only requirement is that the input voltage V_2 must be negative.

→ Hence divider circuits are used at two quadrants circuit of $V_1 \to +ve$, $V_2 \to -ve \Rightarrow$ 2nd Qua

2 Squaring Circuit (Λ^2)



$V_0 = K(V_1)^2$

→ The squaring circuit gives square of the input voltage (V_1) applied.

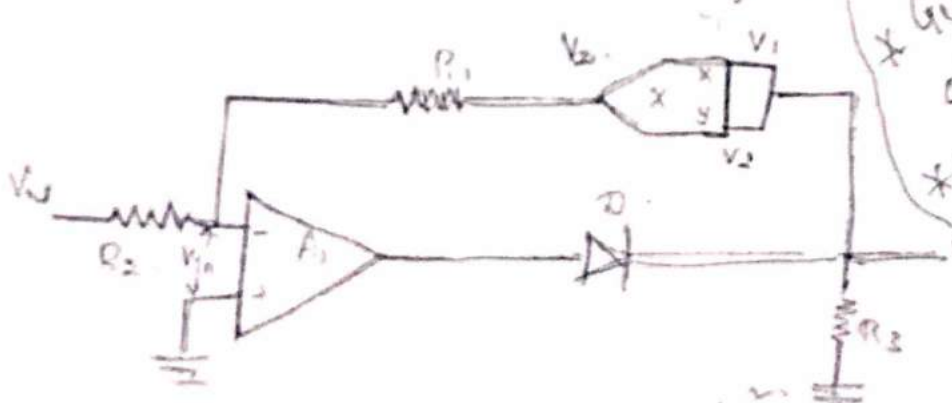
→ The multiplier inputs are connected together to get the squaring circuit as shown in fig.

→ The same signal (V_1) is applied to both the input terminals of the multiplier so $V_2 = V_1$ and hence the output of the multiplier is

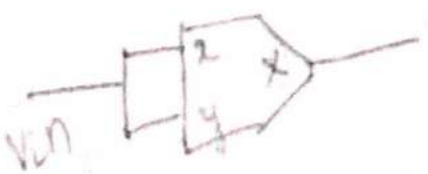
$$\boxed{V_0 = K V_1 V_2 = K V_1^2}$$

Square Rooting Circuit ($\sqrt{\ }$)

The circuit is shown in fig.



$V_0 = V_{in}^2$



$V_0 = K V_{in}^2$

* same i/p V is applied in both terminals of a multiplier
* Gives a square of the i/p V.
* multiplier i/p are connected together to get squaring circuit.
* And o/p V is $V_0 = V_{in}^2$

20)

→ A multiplier configured as Squaring circuit is used in the feedback loop. The gain of the opamp is A_1 is say A and voltage between -ve and the terminal is V_{in}.

→ So we can write. (gain of the op amp)

$$V_o = -V_{in} \times A \quad ; \quad V_{in} = -\frac{V_o}{A} \rightarrow (1).$$

→ Now, the voltage (V_{in}) is composed of two components one that of V_Z and other that of V_N.

$$\boxed{V_{in} = V_Z + V_N}$$

→ By using Superposition principle, the.

$$V_{in} = V_N \times \frac{R_1}{R_1+R_2} + V_Z \times \frac{R_2}{R_1+R_2} \rightarrow (2).$$

But, $V_Z = K V_1 V_2 = K V_o^2$. $\{ V_1 = V_2 = V_o \}$

$$\therefore V_{in} = V_N \frac{R_1}{R_1+R_2} + K V_o^2 \frac{R_2}{R_1+R_2} \rightarrow (3).$$

Equating (1) & (3),

$$-\frac{V_o}{A} = V_N \frac{R_1}{R_1+R_2} + K V_o^2 \frac{R_2}{R_1+R_2}.$$

$$-\frac{V_o}{A}(R_1+R_2) = V_N R_1 + K V_o^2 R_2.$$

$$V_o^2 = \frac{-\frac{V_o}{A}(R_1+R_2) - V_N R_1}{K R_2}$$

$$V_o^2 = -\frac{V_o}{AK} \times \frac{R_1+R_2}{R_2} - \frac{V_N R_1}{K R_2}$$

Now A is high, the term

$\frac{-V_o (R_1+R_2)}{A K R_2} << 1$, hence it is neglected.

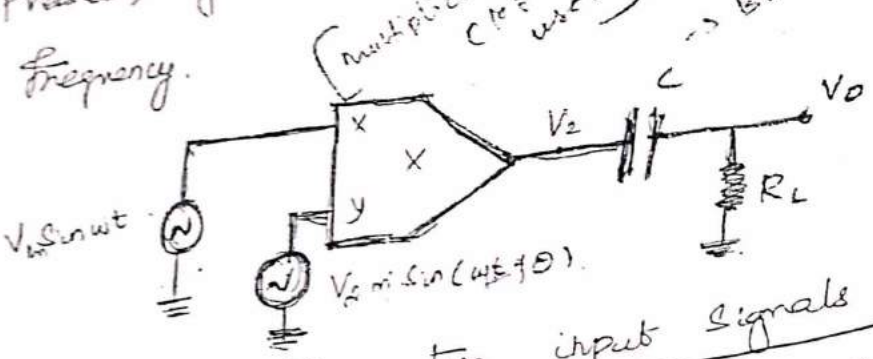
$$V_o^2 = -\frac{V_N R_1}{K R_2}$$

$$\boxed{V_o = \sqrt{(-V_N)\frac{R_1}{K R_2}}} \rightarrow (4).$$

→ As seen from eqn (4), the output is proportional to the square root of V_N, but the V_N must always be negative ($V_N < 0$), otherwise the circuit, otherwise the circuit becomes latched up and normal operation can only be restored by breaking the feedback loop. To avoid such a problem, a series diode (D) is provided.

9m FREQUENCY DOUBLER

→ The multiplication of two sinewaves of same frequency, but possibly different amplitudes and phases, gives us a signal of a double frequency.



→ Consider the two input signals as,

$V_1 = V_{1m}\sin\omega t$ and $V_2 = V_{2m}\sin(\omega t+\theta)$

When the two inputs are given to a multiplier we get, $V_o = K V_1 V_2$ ← General Eqn of Multiplier o/p

$V_o = K V_{1m}\sin\omega t \; V_{2m}\sin(\omega t+\theta)$.

$= K V_{1m}V_{2m}\sin\omega t \sin(\omega t+\theta)$. { $\sin(a+b) = \sin a\cos b + \cos a\sin b$ }

multiply & divide (2)

$= \frac{K V_{1m}V_{2m}}{2}\cdot\left[2\sin\omega t(\sin\omega t\cos\theta + \cos\omega t\sin\theta)\right]$

$= \frac{K V_{1m}V_{2m}}{2}\left[2(\sin^2\omega t\cdot\cos\theta) + 2\sin\omega t\cos\omega t\sin\theta\right]$

{ $\sin^2\theta = 1-\cos 2\theta$ } { $2\sin\theta\cos\theta = \sin 2\theta$ }

$= \frac{K V_{1m}V_{2m}}{2}\left[2\left(\frac{1-\cos 2\omega t}{2}\right)\cos\theta + \sin 2\omega t\sin\theta\right]$

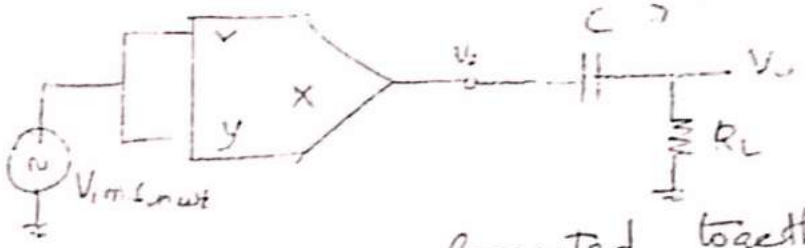
{ $\sin^2\theta = \frac{1-\cos 2\theta}{2}$ }

$$V_o = \frac{K V_{1m} V_{2m}}{2} \left[\cos\theta - \cos 2\omega t \cos\theta + \sin\omega t \sin\theta \right]$$

$$V_o = \frac{K V_{1m} V_{2m}}{2} \cos\theta - \frac{K V_{1m} V_{2m}}{2} \cos(2\omega t + \theta)$$

⇒ The first term is DC for a phase difference of θ, while the second term varies with time but at twice the frequency of the inputs. Thus circuit acts as a frequency doubler.

⇒ Such a frequency doubler can be obtained by using a squaring circuit as shown in fig



⇒ The two inputs are connected together hence

$$V_1 = V_2 = V_m = V_m \sin\omega t$$

Here $\theta = 0°$, which is phase difference between the two inputs.

$$\sin^2\omega t = \frac{1 - \cos 2\omega t}{2}$$

$$V_2 = K V_m^2 = K (V_m \sin\omega t)^2$$

$$= K V_m^2 \left(\frac{1 - \cos 2\omega t}{2}\right) \quad \text{as } \sin^2\omega t = \frac{1 - \cos 2\omega t}{2}$$

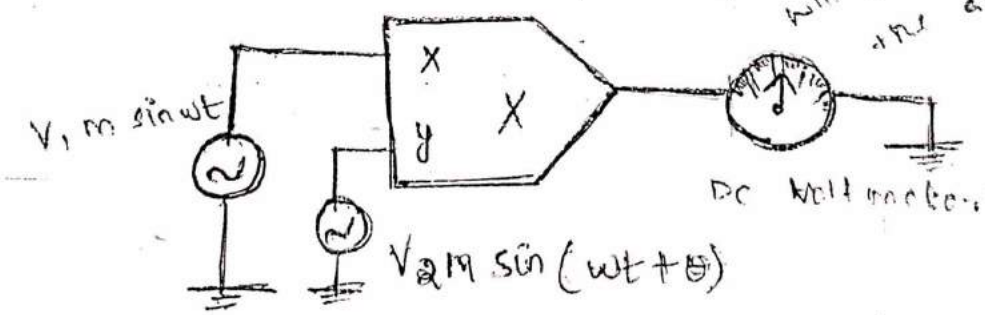
$$V_o = \frac{K V_m^2}{2} - \frac{K V_m^2 \cos 2\omega t}{2}$$

* The o/p of the multiplier is the sum of DC signal with time varying signal of double the input frequency.
* The capacitor (C) connected in series with the o/p block the DC and removes it. Thus we get

$$V_o = \frac{K V_m^2}{2} \cos 2\omega t$$

Phase Angle detection :-

The frequency doubler circuit with two inputs of same frequency, but different amplitudes and phases can be used to obtain the phase angle detection circuit as shown in the fig.



The o/p of the multiplier is

$$V_o = \frac{K V_1 m V_{2m} \cos\theta}{2} - \frac{K V_{1m} V_{2m}}{2} \cos(2\omega t + \theta)$$

* The voltmeter will not respond for ac component present in the o/p, while the dc component can be easily measured on the voltmeter.

Now for $\theta = 0^\circ$, Voltmeter reading = $\frac{K V_{1m} V_{2m}}{2}$ ($\cos\theta = \cos 0 = 1$)

For $\theta = 45^\circ$, voltmeter reading = $\frac{K V_{1m} V_{2m}}{\sqrt{2}}$ ($\cos\theta = \cos 45 = \frac{1}{\sqrt{2}}$)

$\theta = 90^\circ$, " $V_0 = 0$ ($\cos\theta = \cos 90 = 0$)

$\cos 0^\circ = 1$
$\cos 45^\circ = \frac{1}{\sqrt{2}}$
$\cos 90^\circ = 0$

Calibrating the dc voltmeter as a phase angle meter : the phase angle b/w the 2 i/p's can be measured.

Key Points :

* voltage divider $V_0 = -\frac{V_{IN}}{KV_2}$
* Squaring circuit $V_0 = K V_1 V_2$
* Square rooting circuit $V_0 = \sqrt{(-V_N)\frac{R_1}{KR_2}}$
* Frequency doubler $V_0 = \frac{K V_m^2}{2} \cos 2\omega t$
* phase angle detection $V = \frac{K V_{1m} V_{2m}}{2}$

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TITLE: Phased locked loop and closed loop analysis.

OBJECTIVE: The students should be able to learn about PLL and closed loop analysis

APPLICATIONS:

MC12040 logic network (Motorola)

UNIVERSITY QUESTIONS:

1. State the operation of a basic PLL. (May/June-14) (2 mark)
2. Define Pull in time as referred to PLL. (NOV/DEC-15) (2 marks)

NOTES

3. Draw the basic schematic of the PLL and explain its operation (NOV/DEC-16) (16 marks)

Phased locked loop (PLL).

Introduction :-

* PLL is also called a closed loop feedback system, whose o/p frequency and phase are in lock with the frequency and phase of the input signal.

$$f_o \text{ \& } \phi_o \overset{\text{lock}}{=} f_i \text{ \& } \phi_i$$

* The PLL is an important building block of a linear system, which can detect the phases of & signals and reduce the difference in the presence of a phase difference.

* The realization of PLL had been very costly in most industrial and consumer applications

* Monolithic IC Technology has made the fabrication of IC PLL inexpensive and the use of PLL is constantly expanding in many application such as

Satellite communication, FM demodulation, stereo demodulation, tone detectors and frequency synthesizers.

OPERATION of PLL

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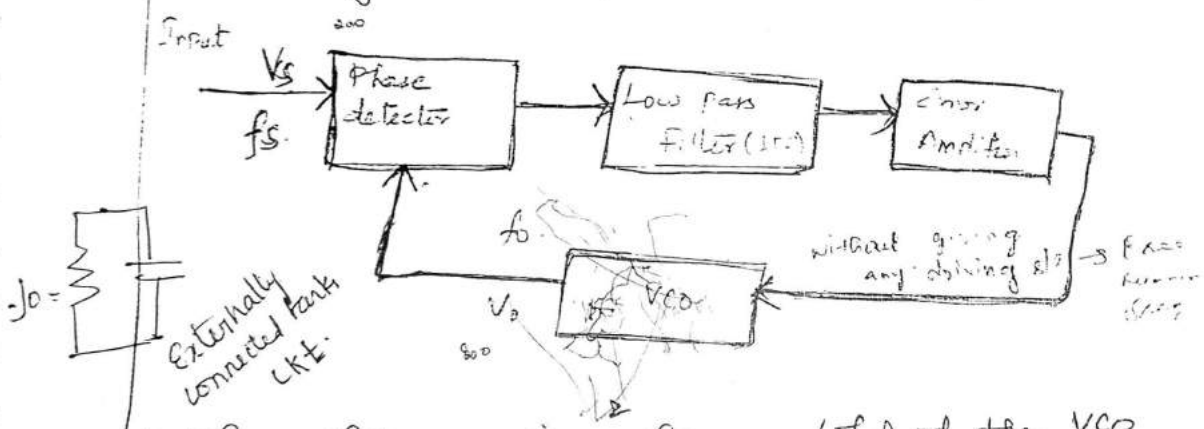
→ The basic block diagram of a phase locke loop is shown in fig. The main elements of the PLL are a phase detector / Comparator, a loo pass filter, an error amplifier (A) and a Voltage Controlled oscillator (VCO).

→ The phase detector is fundamentally a multiplier which generates the sum and difference of the two input signals. ①



→ The free running frequency (fo) of the VCO is determined by an externally connected resistor and a timing capacitor.

→ When the loop is locked, the frequency (fo) is directly proportional to an externally applied Voltage (Vc), called the dc control Voltage.

$f_o \propto V_c$ ③

→ When an input Periodic Signal (V_i) of frequency (f_i) and VCO output signal (V_o) of frequency (f_o) are applied to the PLL, the phase detector produces a dc (or) low frequency signal (V_c) which is proportational to the phase difference between the input signal (V_i) and the VCO o/p signal (V_o)

→ When the phase sensitive signal from the phase detector is passed through the low pass filter F(S), the high frequency sum component is filtered out.

→ The low frequency different component passes out of filter and then amplified by an error amplifier (A).

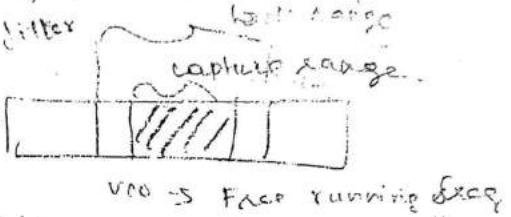
⇒ This amplified signal is applied to the input of VCO as control voltage (V_c), which changes the VCO frequency (f_o) in such a way that the difference between f_o and f_i is reduced.

→ If two frequencies are brought almost identical by this feedback action, then the circuit is to be locked. (R)

2#1

→ Once the lock is received, the VCO frequency f_0 becomes equal to the input signal frequency (f_i) with a finite phase difference

Q. ... od as a bandpass filter it eliminate noise, interference



PROCESS of CAPTURE

→ In the unlocked Condition of the PLL, the VCO operates at a frequency (f_c) called Center frequency (or) free running frequency.

→ This corresponds to an applied voltage of 0V dc at its control input.

→ Let us assume that the feedback loop of the PLL is initially open between the loop filter and VCO control input.

→ An input signal of frequency (f_i), which is assumed to be closer to the VCO center frequency (f_c) is applied to the input of phase detector.

→ The phase detector is usually an analog multiplier that multiplies the two

 signals.

→ The phase detector is usually an analog multiplier that multiplies the two sinusoids together and it produces the sum and difference of the two signals at its output.

→ Since the high frequency sum component is filtered out by LPF, the output of the LPF is a sinusoid, whose frequency is equal to the difference between the VCO center frequency (f_c) and incoming signal frequency (f_i).

→ The difference frequency sinusoid is applied to the VCO input as the control voltage (V_c). Thus, this will make the VCO frequency (f_o), a sinusoidal function of time.

→ The output frequency of the phase detector, the difference between f_o and f_i moves to a lower frequency. When f_o moves closer to f_i and moves to a higher frequency when f_o moves far away from f_i.

$f_{oc} = \frac{d\theta_e}{dt}$

→ It reflects in the phase detector output having an asymmetrical waveshape during the Capture process is shown in fig.

→ This asymmetry waveform produces a dc Component which in turn shifts the VCO frequency fo towards fi and the difference gradually decreased.

→ When the loop is locked, the frequency difference is zero, and a dc voltage remains at the loop filter output.

→ Once lock is achieved, the VCO can track the signal will beyond the capture range. Reducing the Bw of the filter thus improves the rejectivity of out of band signals but it reduces the capture range, the pull in time increases and the phase margin become less.

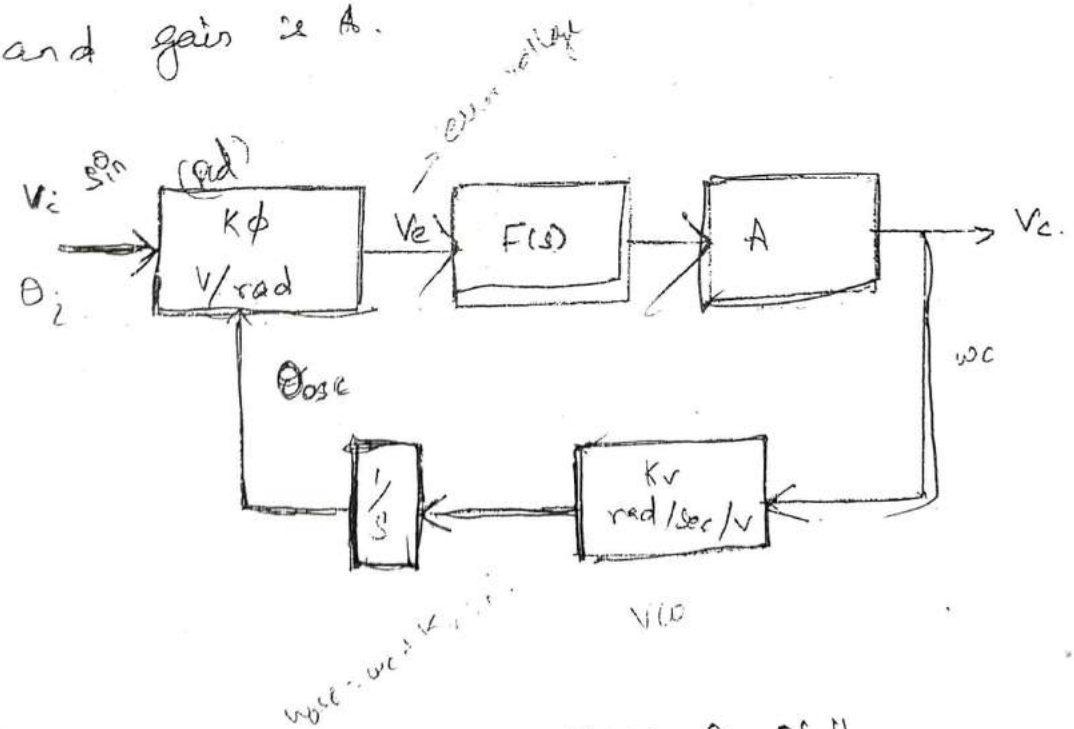
→ The Capture Range is defined as the range of inputs frequencies around the center frequency within which the loop can get locked from an unlocked condition.

→ The Pull in time is the total time required for the loop to get captured with the input signal.

CLOSED LOOP ANALYSIS of PLL:

⇒ The block diagram is shown in fig. is used to study the closed loop analysis of PLL.

→ Assume that the PLL is initially in locked condition and the gain of phase detector is K_ϕ Volts/rad of phase difference, the transfer function of the loop filter is F(s) and gain is A.



→ The input sinusoidal signal (V_i) is represented by.

$$V_i = V_p \sin(\omega t + \theta_i). \rightarrow (1)$$

→ If the phase shift of the signal at the VCO output is θ_{osc}, then the average value of the output of the phase detector is

$$V_e = K_\phi (\theta_i - \theta_{osc}) \rightarrow (2)$$

→ The phase of VCO signal output = The integr of VCO output frequency.

and it can be expressed as.

$$\omega_{osc}(t) = \frac{d\theta_{osc}(t)}{dt}$$

$$\theta_{osc}(t) = \int_0^t \omega_{osc}(t)\, dt + \theta_{osc}/_{t=0} \rightarrow (3)$$

→ The integral component is represented by 1/S inside the VCO block.

→ The dc control voltage (V_c) is the input to VCO and the output frequency of VCO are related as

[where ω_c = center frequency when $V_c = 0$]

$$\omega_{osc} = \omega_c + K_v V_c \rightarrow (4).$$

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→ Then the closed loop transfer function of the PLL becomes

$$\frac{V_c(s)}{\theta_i(s)} = \frac{K_\phi F(s) A}{1 + K_\phi F(s) A \frac{K_V}{s}}$$

$$= \frac{s K_\phi F(s) A}{s + K_\phi F(s) A K_V}$$

→ The response of the loop to frequency variations at the input rather than phase, the above equation can be represented as,

$$\frac{V_c(s)}{\omega_i(s)} = \frac{V_c(s)}{s\theta_i(s)} = \frac{K_\phi F(s) A}{s + K_\phi F(s) A K_V}$$

Since, $\omega_i(s) = \frac{d(\theta_i(s))}{dt}$ & $\omega_i(s) = s\theta_i(s)$.

↳ Considering $F(s) = 1$ with the loop having a first order low pass frequency response, we have,

$$\frac{V_c(s)}{\omega_i(s)} = \frac{K_\phi A}{s + K_\phi K_V A} = \frac{K_b}{s + K_b} \times \frac{1}{K_V}$$

where K_b is the loop bandwidth is given by $K_b = K_\phi A$. K_V is the effective BW, the loop and capture ranges are very much dependent on K_V, the

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and the capture range reduces.

* Therefore the property of interference rejection improves.

Key Points :-

* Operation of PLL
* Process of capture
* closed loop analysis of PLL.

$$\frac{V_c(s)}{V_i(s)} = \frac{K_\phi A}{S + K_\phi K_V A}$$

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PAGE NO: 9.19
UNIT: III
CLASS NO: 26

TITLE: Voltage Controlled oscillator

OBJECTIVE: The students should be able to learn about the VCO design and waveform.

APPLICATIONS:

Telcordia GR-1244 Core states

UNIVERSITY QUESTIONS:

1. Draw the block diagram of IC 566 VCO. (Nov/Dec-16) (2 marks)
2. Explain the application of VCO for FM generation. (Apr/May-15) (16 marks)

NOTES

3. Draw the Block diagram of VCO and explain its operation. Also derive the frequency of oscillator. (Nov/Dec-13) (16 marks)
4. Describe how a PLL could be used as a VCO. (Nov/Dec-15) (8 marks)

Voltage Controlled Oscillator:-

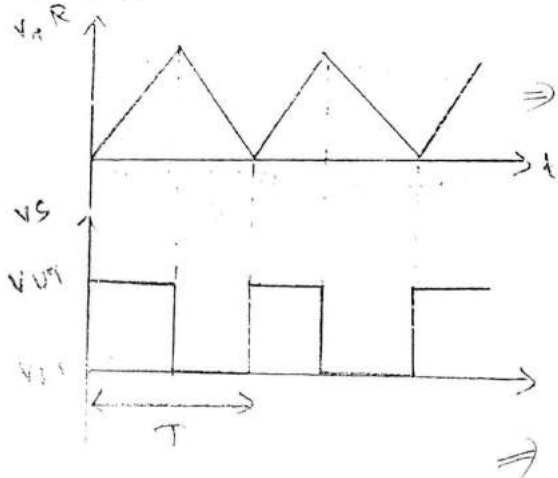
An oscillator whose frequency is controlled by an external voltage is known as a VCO.

* A voltage Controlled oscillator is (an oscillator circuit) in which the frequency of (oscillation can be controlled) by an externally (applied voltage).

* The VCO provides the linear relationship between the applied voltage and the oscillation frequency.

⇒ Linear Relation b/w applied voltage & frequency

Waveform :-



⇒ It is also called Voltage to freq conversion (OR) Voltage to freq conversion.

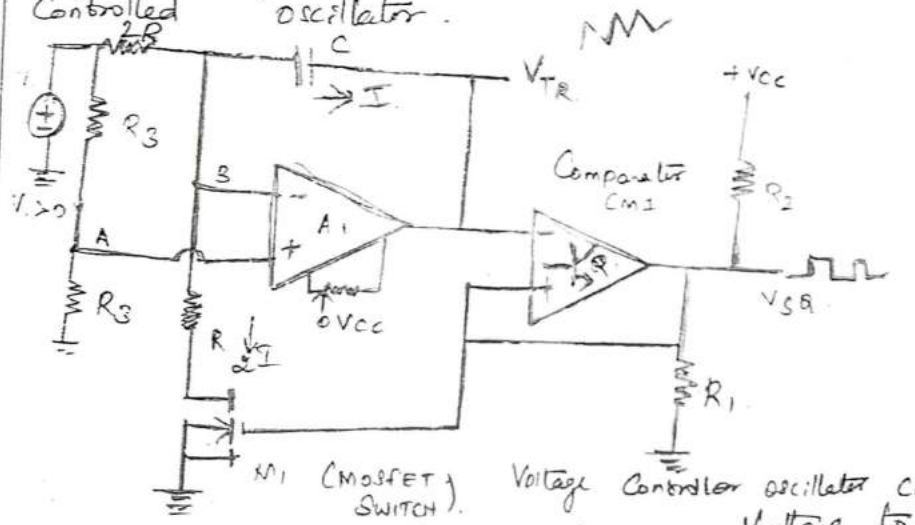
⇒ Applied voltage called control voltage.

* $A_1 \rightarrow$ V to I conv
* $C \propto V_i$

→ (Applied Voltage is Called Control Voltage). The Control of frequency with the help of control Voltage is also called (Voltage to frequency Converter) Hence VCO is Called (Voltage to frequency Converter)

→ Practically, VCO is used to produce (Square) and (triangular) waveforms, whose frequency is Controlled by control Voltage.

→ The fig shows the opamp based Voltage Controlled oscillator.



Voltage Controlled oscillator ckt.

→ In this circuit, opamp (A_1) is Voltage to Current Converter, it forces the current through Capacitor 'C' which is linearly proportational to the input Voltage (V_i). $C \propto V_i$

→ For getting triangular & Square waveform, Capacitor must change and discharge and this current direction through Capacitor must keep on alternating.

"C" is controlled by MOSFET

Cmp = low, M1 is off, R is floating

Cmp = high, M1 is on, R is ground

↳ The direction of Current through 'C' is controlled by MOSFET Switch (M_1)

↳ It is driven by Schmitt trigger Comparator (Cmp).

CMP low, M_1 - off, R - floating

CMP high, M_1 - on, R - grd

↳ When the output of Cmp is low, M_1 is off and resistance (R) remains floating, while when the output of Cmp is high, M_1 is on and resistance (R) gets connected to the ground.

V_{TR} - /\/\/\, V_{SQ} - ⊓⊓

↳ The Square wave is Obtained at terminal V_{SQ} & The triangular wave is obtained at terminal V_{TR}.

R_1 - ON, V_{CE} - Sat ⇒ 0

↳ When output transistor (Q) is on, V_{SQ} ∝ $V_{CE(sat)}$ = 0 which is equal to zero. Q_1 - OFF, V_{SQ}

↳ While when (Q) is off, then V_{SQ} is directly decided by Voltage divider of R_1 and R_2.

$$V_{SQ} = V_{CC} \times \frac{R_1}{R_1 + R_2}$$ → when Q is off.

→ As the output (V_{SQ}) is Connected to the non-inverting terminal of Comparator (CMP), the high and low values of the V_{SQ} are the upper and lower threshold levels of Comparator (Cmp).

V_{SQ} high, low

comp o/p - V_{UT}, V_{LT}

VSQ → high (on) low

Tr ... ...low.

→ Due to voltage divider of R_3 & R_3, the voltage at node A is

$$V_A = V_i \times \frac{R_3}{R_3 + R_3} = V_i \frac{R_3}{2R_3} = \frac{V_i}{2} \rightarrow (1).$$

→ Due to the virtual ground, $(V_B = V_A)$

$$\boxed{V_B = \frac{V_i}{2}} \rightarrow (2).$$

→ Thus the current through 2R resistor is.

$$\boxed{I = \frac{V_i - V_i/2}{2R} = \frac{V_i}{4R}} \rightarrow (3).$$

Through 2R
$I = V_i - V_B/2R$
$= \frac{V_i - V_i/2}{2R}$
$= \frac{V_i}{2R} - \frac{V_i}{4R}$
$I = \frac{V_i}{4R}$

→ The Eqn (3) shows the opamp (A1) acts as Voltage to Current Converter.

→ Assume that the output VSQ is low, hence M_1 is off and the resistance R is floating. So entire current $I = \frac{V_i}{4R}$ has to pass through the capacitor and the voltage (V_{TR}) starts decreasing due to polarity of voltage across capacitor. So V_{TR} ramps down.

Due to opamp
VSQ → low
M is off
R is floating
VTR decreasing

IF VSQ low, M_1 - OFF, R - Floating = $\frac{V_i}{4R}$ through
V_{TR} - decreases, ramp

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VTR becomes zero, Cmp is ON, VSQ is high, M is ON, R is ground, VTR is increasing

→ When V_{TR} becomes zero, then Comparator (CMP) changes its state and output V_{SQ} becomes high. Due to this M, becomes on and the resistance (R) gets connected to the ground. The current through resistance (R) is thus, V_{TR} - 0, cmp - high, M_1 - ON, R Gnd

mul & divi 2

$$\boxed{I_R = \frac{V_B}{R} = \frac{V_i}{2R} = 2 \times \frac{V_i}{4R} = 2I} \rightarrow (4)$$

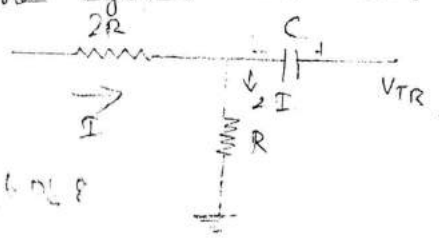
ramp up

→ Now current (I) out of 2I is supplied by resistance 2R. but remaining current (I) must be supplied by capacitor as shown in fig.

→ Thus the direction of current through the 'C' reverses. Hence V_{TR} starts ramping up i.e starts increasing. It can be noted that capacitor current (I) gets hence triangular waveform is available at V_{TR}.

→ As soon as V_{TR} reaches the level of V_{SQ}, the comparator changes its state making M_1 off.

→ Thus, the current (I) through capacitor again reverses its direction and V_{TR} ramps down. Thus the cycle continues.



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Period of oscillation:-

The period of oscillation is determined by equating the change expressions.

$$C\frac{dv}{dt} = I$$

$$\therefore C\Delta V = I\Delta t$$

During half cycle,

$$\Delta v = V_{UT} - V_{LT}; \quad I = \frac{V_i}{4R}$$

and $\Delta t = \frac{T}{2}$

$$C(V_{UT} - V_{LT}) = \frac{V_i}{4R} \times \frac{T}{2}$$

$$T = \frac{4RC \times 2(V_{UT} - V_{LT})}{V_i}$$

$$F = 1/T = K_V V_i \rightarrow (5) \qquad F \propto V_i$$

where, $K_V = \frac{1}{4RC \times 2(V_{UT} - V_{LT})} \rightarrow (6)$

The eqn (5) shows that the o/p frequency is linearly proportional to the i/p voltage and thus circuit works as VCO.

Limitations:-

* The accuracy of such vco circuit is limited because of speed of response of opamp Comparator and MOSFET switch.

* ~~Error~~ is caused at low frequencies due to i/p bias current and the offset voltage of op-amp (A_1).

* The Non-Zero channel resistance of M_1 when it is on i.e $r_{ds(on)}$ is another factor causing an error. Hence in practice integrated version of vco is used.

Key Points:-

* $I_R = \frac{V_B}{R} = \frac{V_i}{2R} = 2 \times \frac{V_i}{4R} = 2I$

* Period of oscillation

$$T_r = \frac{1}{4RC \times 2(V_{UT} - V_{LT})}$$

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PAGE NO: 227
UNIT: III
CLASS NO: 27

TITLE: Monolithic PLL IC 565

OBJECTIVE: The students should be able to learn about the monolithic PLL IC 565 circuit and working.

APPLICATIONS:

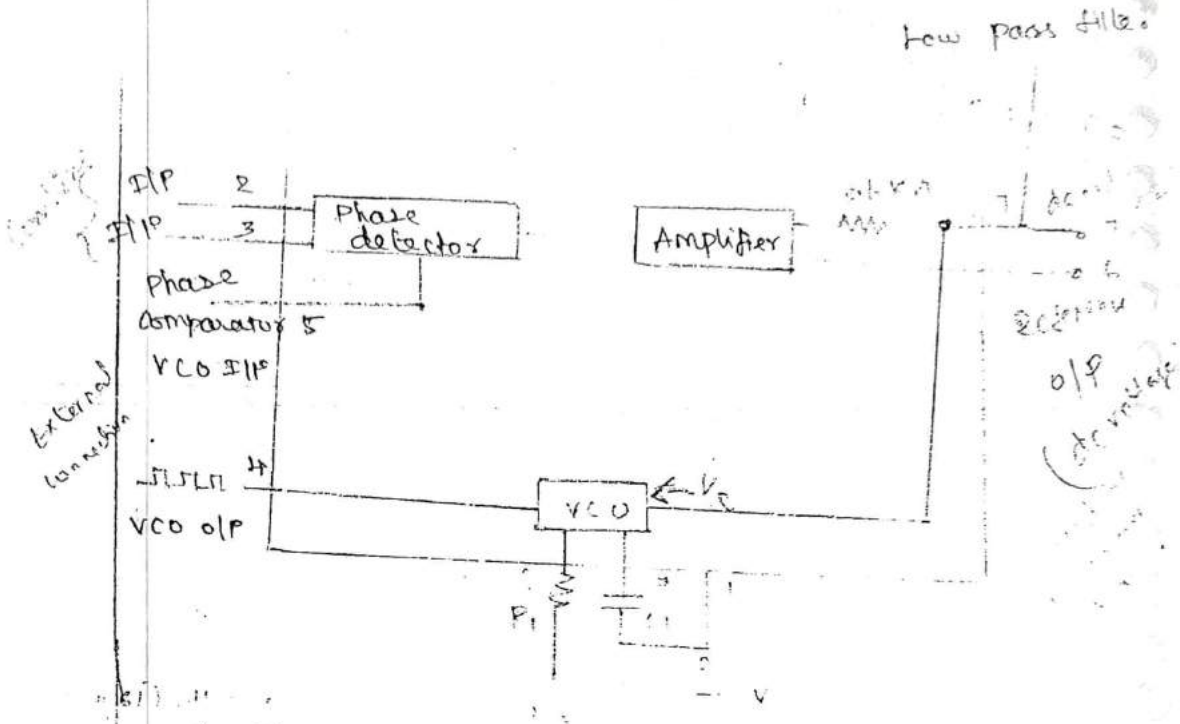
Intel 0.18μm VLSI Technology

UNIVERSITY QUESTIONS:

1. Enlist any four applications of NE565 PLL. (Nov/Dec-16) (2 marks)
2. Define the term lock-in-range of PLL (Dec-12) (2 marks)
3. With block schematic explain the working Principle of PLL IC NE 565 (Nov/Dec-16) (12 marks)
8. Define capture range and lock range; derive for Monolithic phased locked loop: LM515 NOTES Capture range and lock range (Apr/May-17) (16 m

* Monolithic PLL's are introduced by signetics as NE/SE 560 series and by National semiconductor as LM560 series. These IC's are differs mainly in operating range, Power supply, frequency and BW requirements.

* IC 565 is 14 pin, DIP Package and 10 pin metal can package.



* It consist of phase detector, amplifier, LPF and VCO. The phase locked feedback loop is not internally connected. It is necessary to connect o/p of VCO (Pin 4) to the phase comparator (Pin 5), externally. In frequency multiplication application a digital divider is inserted b/w Pin 4 and 5

* The Free running (or) center frequency is given by

$$F_c = \frac{1.2}{4R_1C_1} \text{ Hz}$$

, R_1 & C_1 are connected to Pin 8 & 9.

* We can adjust the free running frequency by proper selection of R_1 and C_1

* The lock range and capture range of PLL IC 565 are given by $f_{lock} = \pm \frac{8f_c}{V}$ Hz

and

$$f_{cap} = \pm \left[\frac{f_{lock}}{2\pi (3.6)(10^3)(2)} \right]^{1/2} \quad (2)$$

From Eqn (2), we known that lock range increase with an decrease in input voltage and decreases with an increase in input voltage.

DERIVATION OF LOCK IN RANGE.

→ Assume (ϕ) radians is the phase differen between the input signal and Vco Voltage

→ Then the output voltage of phase detector (V_e → error voltage) is given by.

$$V_e = K_d \left(\phi - \frac{\pi}{2} \right) \rightarrow (1).$$

K_d → phase angle to voltage Transfer Co-efficient of phase detector.

→ Therefore, the Control Voltage (V_c) of Vco is

$$V_c = A \cdot V_e$$

$$V_c = AK_d \left(\phi - \frac{\pi}{2} \right) \rightarrow (2).$$

Where, A is the Voltage gain of error amplifier, The V_c shifts the Vco frequency from f_c to f represented by.

$$f = f_0 + k_0 V_c \rightarrow (3).$$

→ Where, K_o is the Voltage to frequency transfer Co-efficient of VCO.

→ When PLL achieves lock with signal frequency (f_i) we have. $\boxed{f = f_i}$

$$f = f_i = f_o + K_o V_c \rightarrow (4).$$

$$\therefore V_c = \frac{f_i - f_o}{K_o} \rightarrow (5).$$

From Eqn (2) & (5), we get.

$$V_c = \frac{f_i - f_o}{K_o} = A K_d \left(\phi - \frac{\pi}{2}\right).$$

$$\phi = \frac{f_i - f_o}{A K_o K_d} + \frac{\pi}{2}.$$

$\phi = ?$ if $V_c = 0$

→ The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radians as shown in fig and $\boxed{V_{c(max)} = \pm K_d \frac{\pi}{2}}$. Then, the Corresponding Value of the maximum Control Voltage available to drive the VCO is given by.

$$\boxed{V_{c(max)} = \pm \frac{\pi}{2} K_d A}$$

→ The max VCO swing in frequency is given by 23!

$$(f-f_0)_{max} = K_0 V_{c\,max} = \pm K_d K_0 A\left(\frac{\pi}{2}\right)$$

→ where $(f-f_0)_{max}$ is considered as the max deviation frequency from center frequency (f_0) of VCO.

→ Therefore, the maximum range of signal frequency over which the PLL can remain locked will be

$$f_i = f_0 \pm (f-f_0)_{max}.$$
$$= f_0 \pm K_d K_0 A\left(\frac{\pi}{2}\right) = f_0 \pm \Delta f_L.$$

→ The Lock-in frequency range is $= 2\Delta f_L$ and from the above eqn, it is given by $\Delta f_L = K_d K_0 A\left(\frac{\pi}{2}\right)$

$$\text{Lock in range} = 2\Delta f_L = K_d K_0 A \pi = K_v \pi.$$

where, $K_v = K_d K_0 A$ is the loop bandwidth for.

PLL IC 565, the $K_0 = \frac{8 f_0}{V}$.

where, $V = +V_{CC} - (-V_{CC})$ & $K_d = \frac{1.4}{\pi}$; $A = 1.4$

$$\Delta f_L = K_d K_0 A \frac{\pi}{2} = \pm \frac{8 f_0}{V} \times \frac{1.4}{\pi} \times 1.4 \times \frac{\pi}{2}$$

∴ Δf_L is the lock in range becomes

$$\pm 7.8\, f_0 / V.$$

DERIVATION OF CAPTURE RANGE

→ When PLL is not initially locked to the signal, the frequency of the VCO will be its free running frequency (f_o). The phase angle difference between the input signal and the VCO o/p voltage will be.

$$\phi = (\omega_i t + \theta_i) - (\omega_o t + \theta_o)$$

$$= (\omega_i - \omega_o) t + \Delta\theta \rightarrow (1).$$

→ Thus, the phase angle difference does not remain constant using Eqn (1), it will change with time at a rate given by.

$$\frac{d\phi}{dt} = \omega_i - \omega_o.$$

→ The phase detectors output voltage will not have a dc component (using filter capacitor) but will produce an ac voltage with a triangular waveform of peak amplitude $K_d \frac{\pi}{2}$ and a fundamental frequency $(f_i - f_o) = \Delta f$.

→ The LPF is a simple RC Network having the transfer function

$$T(f) = \frac{1}{1 + j f/f_1}.$$

→ The fundamental frequency term supplied to the LPF by the phase detector will be the frequency difference $|\Delta f = f_i - f_o|$, if $\Delta f >$ the LPF transfer function will be approximately,

$$T(\Delta f) = f_1/\Delta f = f_1/(f_i - f_o).$$

→ The voltage (V_c) to drive the VCO is.

$$V_c = V_e \times T(f) \times A.$$

and $V_{c(max)} = V_{e(max)} \times T(f) \times A.$

$$V_{c(max)} = \pm K_d \frac{\pi}{2} \times A \times \frac{f_1}{\Delta f} \quad \left[\because V_{e(max)} = \pm K_d \frac{\pi}{2} \right.$$
$$\left. \& T(f) = f_1/\Delta f \right]$$

→ Thus, the corresponding max shift frequency of VCO is

$$(f - f_o)_{max} = K_o V_{c(max)} = K_d K_o \frac{\pi}{2} \times A \times \frac{f_1}{\Delta f}.$$

→ Let $f = f_i$ for the acquisition of signal frequency the max signal frequency range that can be acquired by the PLL is.

$$\Delta f_c = (f_i - f_o)_{max} = \pm K_d K_o \frac{\pi}{2} \times A \times \frac{f_1}{\Delta f_c} \quad \left[\because \Delta f_c = (f_i - f_o)_{max} \right.$$

$$(\Delta f_c)^2 = \pm K_d K_o \frac{\pi}{2} \times A \times f_1.$$

Since $\Delta f_L = \pm K_d K_o \frac{\pi}{2} \times A$, we get.

$$\Delta f_c = \pm \sqrt{f_1 \Delta f_L}$$

→ Therefore, the total Capture range is, (multiply by '2')

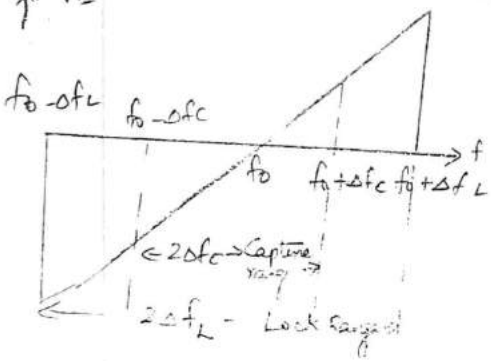
$$2\Delta f_c = 2\sqrt{f_1 \Delta f_L}.$$

$\because \Delta f_L = K_d \cdot K_o \cdot A \cdot \pi/2$

→ Where, the lock in range $= 2\Delta f_L = K_d K_o A \pi = K_v \pi$. In the case of PLL IC 565. $R = 3.6\,k\Omega$, Hence the Capture range is given by. $f = \frac{1}{3.5RC}$

$$\therefore \Delta f_c = \pm \left[\frac{\Delta f_L}{2\pi (3.6)(10^3) C} \right]^{1/2}$$

→ From the fig, we know that, the PLL cannot acquire lock outside the Capture range. Once lock is Captured, it will hold on until the Signal frequency goes beyond the lock in range. In order to increase the lock in range. Larger Capture range is required but it makes the PLL Susceptible to noise. Hence optimization is to be reached. The Lpf BW is large for initial acquisition of signal. When the Signal is Captured, the BW of Lpf is reduced Substantially. This will minimize the interference of Undesirable Signal of Noise.



Key Points :-

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* LM 515 or NE 565 PLL
* Derivation of lock in Range
* Derivation of Capture range.

$$\Delta f_c = \pm \left[\frac{\Delta f_c}{2\pi (3.6)(10^3) C} \right]^{1/2}$$

$$V_c(max) = \pm \frac{\pi}{2} K_d \cdot A.$$

$$K_V = K_d \cdot K_0 \cdot A.$$

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TITLE: PLL Applications Frequency multiplier, Freq. Syn FM demodulator, FS

OBJECTIVE: The students should be able to learn about PLL Applications of FM, FSK, Frequency multiplier, Frequency synthesizer.

APPLICATIONS:

Scanning electron microscopy (SEM) technique

UNIVERSITY QUESTIONS:

1. What is the need for frequency synthesizer? (May/June - 11) (8 marks)
2. Explain the application of PLL as FSK demodulation, FM detection. (May/June-14) (16 mar

NOTES

3. Explain with functional diagram the FSK modulation and demodulation operation using PLLs. (Nov/Dec - 15) (8 marks)

16m

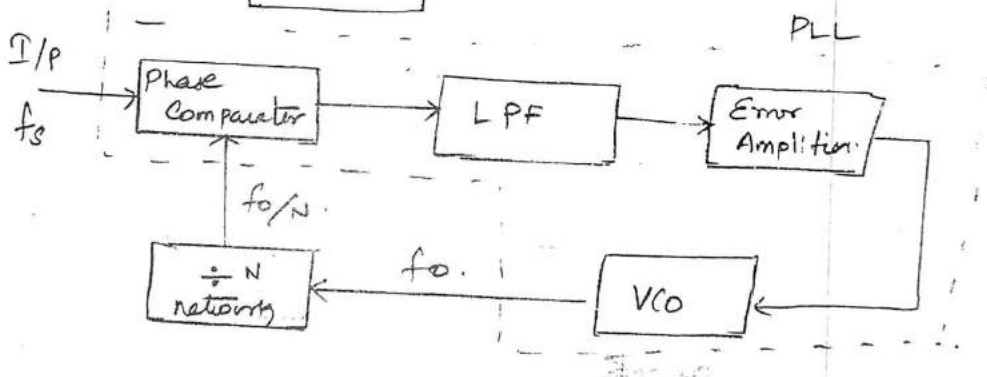
PLL APPLICATIONS:

Frequency Multiplier:- fig shows the block diagram for a frequency multiplier using PLL 565. Here a divide by N network is inserted between the VCO output and the phase comparator input.

→ Since the output of the divider is locked to the input frequency (f_i), the VCO is actually running at a multiple of the input frequency.

→ Therefore, in the locked state, the VCO output frequency (f_o) is given by,

$$f_o = Nf_s$$

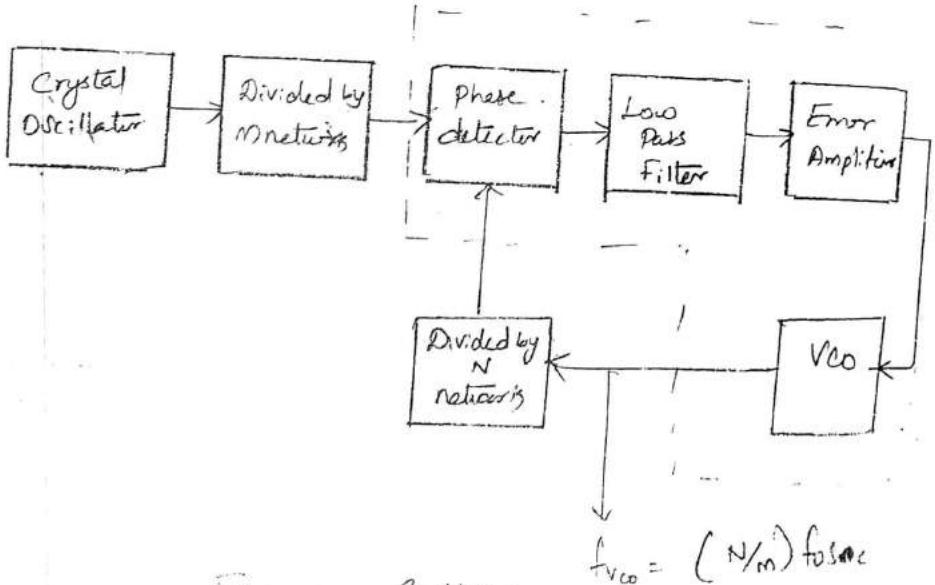


Frequency Synthesizer: The PLL can be used as the basic for frequency synthesizer that can produce a precise series of frequencies that are derived from a stable Crystal Controlled oscillator. The frequency of the Crystal Controlled oscillator is divided by an

* series of freq
* Crystal oscillator → a set of freq that is ÷ by M.

integer factor M by divider network to produce a frequency f_{osc}/M, where f_{SCO} is the frequency of the crystal controlled oscillator. The VCO frequency Vco is similarly divided by factor N by divider network to give frequency equal to f_{VCO}/N. When the PLL is locked in on the divided down oscillator frequency, we will have. $f_{osc}/M = f_{VCO}/N$.

So that, $$f_{VCO} = \left(\frac{N}{M}\right) f_{osc}$$



Frequency Synthesizer

2A1

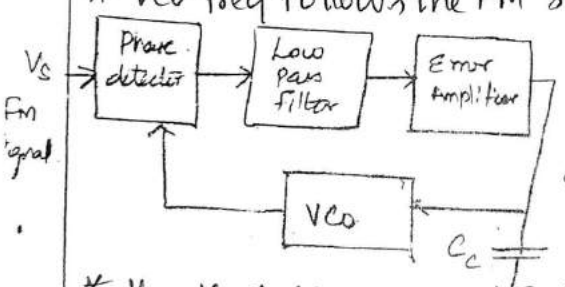
FM Demodulator: The PLL can be very easily used as an FM detector (or) demodulator

→ When the PLL is locked in on the FM signal the VCO frequency follows the instantaneous frequency of the FM signal, and the error voltage (or) VCO control voltage is proportational to the deviation of the input frequency.

change

→ from the center of frequency. Therefore, the ac component of error voltage (or) control voltage of VCO will represent a true replica of the modulating voltage that is applied to the FM carrier at the FM transmitter.

* PLL can be used as a freq modulator
* VCO freq follows the FM sl.



→ The faithful reproduction of modulating voltage depends on the linearity between the instantaneous frequency deviation and the control voltage (VCO).

* Vc or Ve ∝ Δfreq.
* VCO o/p → Exact information of FM signal
* faithfull or Exact information of modulating voltage depends on the linearity b/w VCO & i/p.

→ The FM frequency deviation and the control voltage of VCO should remain in the locking range to produce faithful replica of modulating signal.

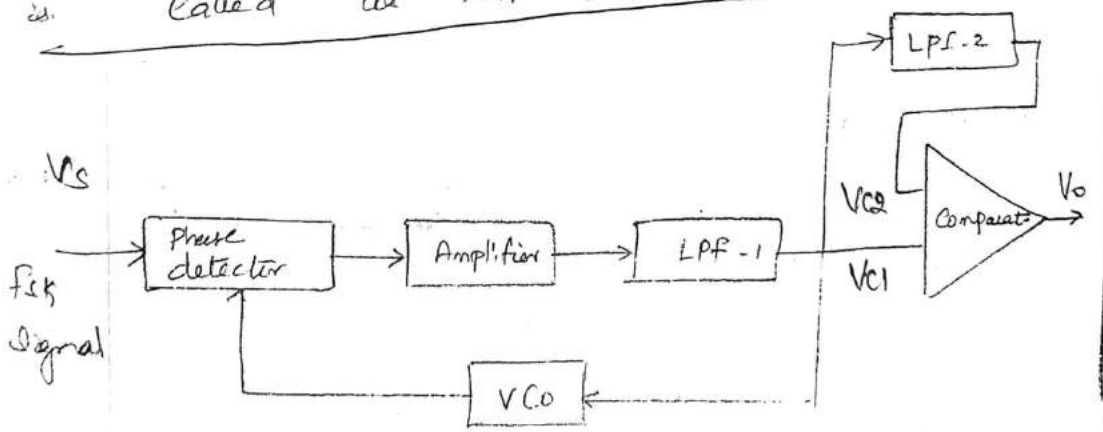
→ Otherwise, the multiplication of these two signals exceeds the $(\Delta f_c)^2$, the VCO will not be able to follow the instantaneous frequency deviation of the fm signal.

Frequency Shift Keying (FSK) Demodulator:

→ In digital data communication, binary data is transmitted by means of a carrier frequency

→ It uses two different carrier frequencies for logic 0 and logic 1 states of binary data signal. This type of data transmission is called frequency shift keying (FSK).

→ In this data transmission, on the receiving end, two carrier frequencies are converted into 1 and 0 to get the original binary data. This process is called as fsk demodulation.



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* PLL can be used as a FSK demodulator. It is similar to the PLL demodulator for analog FM signals except for the addition of a comparator to produce a reconstructed digital o/p signal.

* Consider that there are two frequency one freq (f_1) is represented as '0' and (F_2) " " as '1'.

* If the PLL remain is locked into the FSK signal at both F_1 and F_2, the VCO control voltage which is also supplied to the comparator will be given as,

$$V_{C1} = F_1 - F_0 / K_V$$
$$V_{C2} = F_2 - F_0 / K_V$$

* K_V - the voltage to frequency transfer co-efficient of the VCO.

* The difference between the two control voltage levels will be $\Delta V_C = F_2 - F_1 / K_V$.

* The reference voltage for the comparator is derived from the additional low pass filter and it is adjusted midway blw V_{C1} and V_{C2}.

* Therefore for VC_1 and VC_2 Comparator gives output '0' and '1' respectively

Key Point:-

* Frequency multiplier $\boxed{F_o = N F_s}$
* Frequency synthesizer

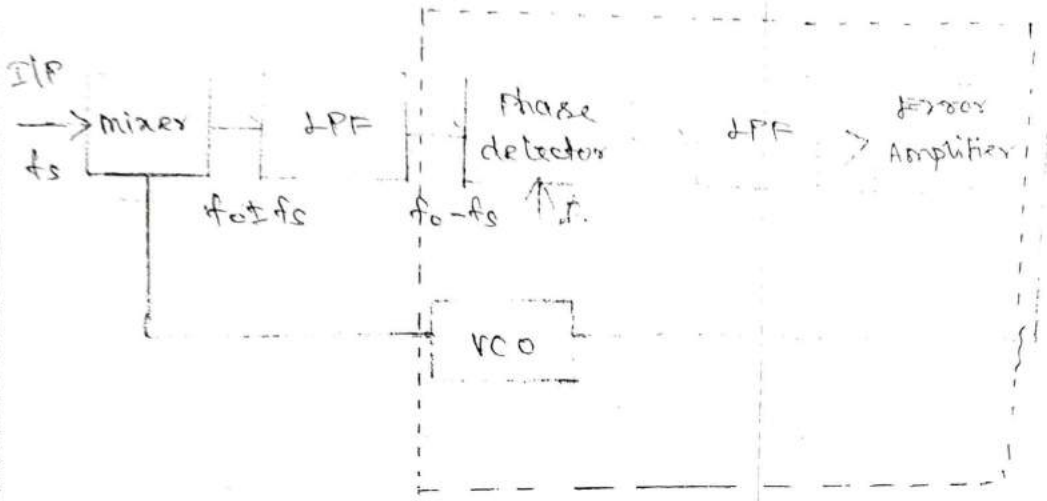
$$\boxed{F_{VCO} = \left(\frac{N}{M}\right) \cdot f_{osc}}$$

* FM demodulator
* FSK demodulator

$$VC_1 = F_1 - F_o \mid K_V$$
$$VC_2 = F_2 - F_o \mid K_V$$

Frequency Translation:

* The frequency translation means shifting the frequency of an oscillator by a small factor



* It consists of mixer, LPF and the PLL.
* the i/p freq (Fo) which has to be shifted is applied to the mixer
* Another inputs to the mixer is the o/p voltage of VCO (Fc)
* The o/p of mixer contains the sum and difference signal ($f_o \pm f_s$).
* The low pass filter connected at the o/p of mixer rejects the ($f_o + f_s$) signal and gives only ($F_o - F_s$) signal at the o/p. The ($F_o - F_s$) signal is applied to the phase detector

* Another i/p for phase detector is the offset frequency (F_1). In the locked mode the VCO o/p frequency is adjusted to make two I/P frequencies of phase detector equal. This gives,

$$F_o - F_s = F_1 \text{ and } F_o = F_s + F_1$$

* By adjusting offset frequency F_1, we can shift the frequency of the osilla to the desired value.

Key Points :-

* AN detection

* Frequency translation

$$F_o - F_s = F_1$$

$$F_o = F_s + F_1$$

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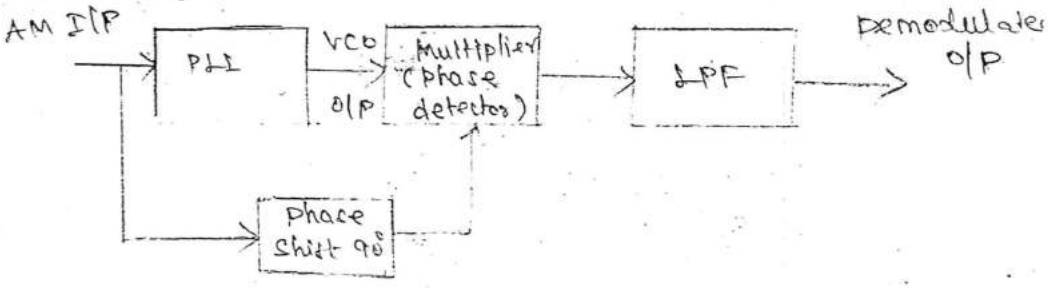
TITLE: AM detection, Frequency Translation

OBJECTIVE: The students should be able to learn about AM detection, Frequency translation
APPLICATIONS: Texas Instrument - LMX 8592 Active
UNIVERSITY QUESTIONS: 1. What are the applications of PLL for AM detection? (Apr/may-15) (2marks) 2. Explain the application of PLL as AM detection (may/June-14) (16marks) NOTES 3. Draw the circuit of a PLL used as AM detector and explain its operation. (Nov/Dec-12) (6 marks) (Nov/Dec-15) (8 marks)

AM detection :

* A PLL can be used to demodulate AM signals



* The PLL is locked to the carrier frequency of the incoming AM signal. Once locked, the o/p frequency of VCO is same as the carrier frequency but it is in unmodulated form.

* The unmodulated signal with 90° phase shift and the unmodulated carrier from o/p of PLL are fed to the multiplier.

* Since VCO o/p is always 90° out of phase with the incoming signal under the locked condition. both the signals applied to the multiplier are in same phase.

* The o/p of a multiplier contains both the sum and difference signals. The LPF connected at the o/p of the multiplier rejects high frequency components gives demodulated o/p.

* As PLL follows the I/P frequencies with high accuracy, a PLL AM detector exhibit a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators